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X-Ray Radiation Effects on CMOS Image Sensor In-Pixel Devices

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1. Introduction

CMOS image sensors (CIS) are now widely applied in a lot of fields from consumer electronics to medical applications due to the advantages over CCD sensors of low power, low cost and high integration capability. As soon as they are utilized in the medical/outer-space applications, radiation tolerance is of great concern. Therefore, a lot of studies have been done on the ionization effects in CMOS image sensors, mainly for 3-Transistor Active Pixel Sensors (3T APS). The conclusion mostly points to the total dose effect on the dark current increase due to oxide trapped charges[1]. However, very few papers have been published on the radiation effects on 4T APS and its in-pixel elementary devices so far. A 4T pixel with pinned photodiode (PPD) and transfer gate (TG) distinguishes itself from its 3T opponent. Thus the previous knowledge about the radiation effect on 3T APS cannot be directly applied to 4T pixels and their in-pixel devices. Furthermore, a special doping profile is used for the in-pixel devices in nowadays commercial 4T image sensors, and they can make a significant impact on the devices' radiation tolerance. The aim of this work is to get an insight on the X-Ray radiation induced degradation mechanism of the in-pixel structures in a commercial 0.18μm 4T APS CIS pixel, and meanwhile trying to provide an effective hardening-by-design technology to finally improve the sensor's radiation tolerance.

2. Radiation Characterization of CIS In-Pixel Devices

Test Structure

In the test structures, several in-pixel devices consisting of pinned-photodiodes, transfer-gate transistors, reset transistors and standard transistors are designed. Fig.1 shows the schematic of a 4T APS structure.

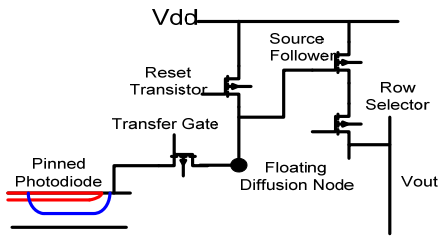


Fig. 1 Schematic of a 4T APS pixel

They were irradiated by an X-Ray source at Philips Health Care at room temperature with a total ionizing dose (TID) level of 31krad, 86krad, 106krad, 109krad and 137krad after 3-turn radiation for different samples. The average energy of this X-Ray source is 46.2keV. During the irradiation, the devices are not biased.

Radiation Degradation on In-Pixel Devices

The in-pixel reset transistor is measured with different voltages applied on the transfer gate, -1V, 1V and 3V, which can switch the transfer gate from off-state to on-state. During the measurement, the substrate is biased at -2.2V in order to turn off the diode included in the design to comply with the design rules (antenna effect). The latter voltage shifts the whole device transfer characteristic due to body effect[2].

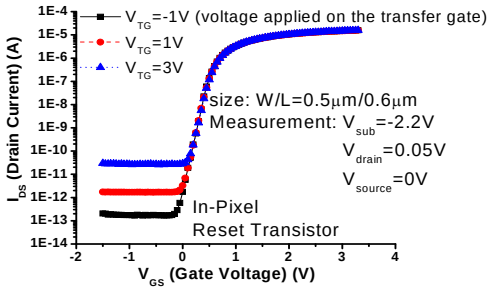


Fig. 2 Transfer characteristic of the in-pixel reset transistor with different voltages applied on the transfer gate

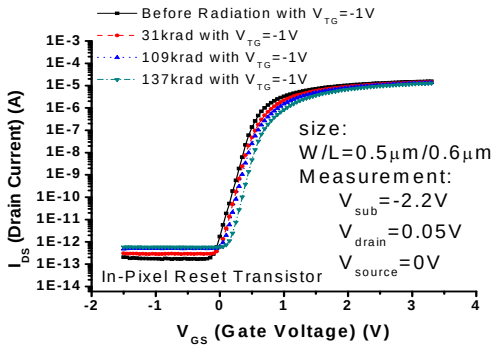
Fig.2 shows the increase of the drain leakage current of the reset transistor with the increase of the voltage on the transfer gate before radiation. Since the transfer gate has an overlapping area with the pinning layer of the PPD which is highly doped, there is a high electric field distribution in that region during the charge transfer[3]. As the voltage increases on the transfer gate node, the electric field is getting higher which will turn the carriers from the PPD to be hot carriers[3] and bombard the interface beneath the transfer gate. In this process, the interface traps are generated and then a leakage path is formed between the floating diffusion node (source node for reset transistor) and the PPD. This leakage path contributes to the increase of the drain leakage current in Fig.2.

Fig.3 shows a positive shift of the whole characteristic after the radiation, which can partially come from the radiation induced interface trap generation inside the reset transistor and transfer-gate transistor. There is another extra implantation layer beneath the reset-transistor gate, thus the X-Ray radiation will introduce some acceptor-like interface trap generation in the lower half of the band gap particularly for the reset transistor[4]. These acceptor-like interface traps will parallel shift the characteristic to the right side and bring the off-state current down, which can be confirmed by a physics model simulation[4][5]. Moreover, the interface trap

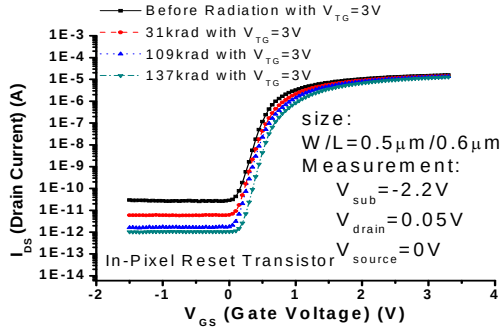
generation will modify the surface potential parameter as well[2]. The threshold voltage of a MOS transistor with a biased substrate can be written as follows:

$$V_T = V_{T0} + \gamma(\sqrt{V_{sub} + 2\phi} - \sqrt{2\phi}) \quad (1)$$

where V_{T0} is original threshold voltage, γ is the body effect parameter, 2Φ is the surface potential parameter, it can be seen that to some extent the surface potential variation will also shift the transfer characteristic parallel to the positive side as illustrated in Fig.3.



(a)



(b)

Fig. 3 Transfer characteristic of the in-pixel reset transistor with different voltages applied on the transfer gate at different TID dose level of 31krad, 109krad and 137krad (a) V_{TG}=-1V, (b) V_{TG}=3V

Meanwhile, in Fig.3 (a) it also shows that the drain leakage current is going up with an increase of the TID dose, which mainly comes from the parasitic leakage path formation due to the trapped charges in the STI oxide[6]. But on one hand the drain leakage current will actually decrease with the positive shift of the threshold voltage described in the previous paragraph[2], and on the other hand, the acceptor-like interface trap generation at the Si-SiO_2 interface can also bring the drain leakage current down after radiation[4]. Nevertheless, in the case of Fig.3 (a) with V_{TG}=-1V, the STI-induced drain leakage current increase is the dominant issue leading to an ultimate drain leakage current increase shown in Fig.3 (a). However, in Fig.3 (b), it is shown that the drain leakage current is decreasing with the increase of the TID level at V_{TG}=3V, and the characteristic is also shifted by the radiation due to the same reasons mentioned previously. But here the leakage current decrease is mostly dominated by the acceptor-like interface trap generation located in the lower half of the band gap. Because of V_{TG}=3V, the pinned-photodiode together with the transfer gate is "connected" with the reset transistor. After the X-Ray damage, not only those acceptor-like interface trap generation in the reset transistor will decline the drain leakage current, but also the same interface trap generation within the PPD and transfer-gate will also contribute to the comprehensive decrease of the drain leakage current of the reset-transistor in the case of transfer-gate turning on[4]. In general, in Fig. 3(b) the interface-trap-induced drain leakage current decrease is dominant over the STI-induced current increase. Therefore, it shows a final drain leakage current decrease in Fig. 3(b).

3. Conclusion

The X-Ray induced degradation of the 4T in-pixel devices mainly shows the variation of the leakage current as well as the unique threshold voltage shift. It is found that the Si-SiO_2 interface trap generation and charge trapping of the shallow trench isolation oxide are the main failure mechanisms behind the leakage current variation. Acceptor-like interface trap generation is a major factor for the in-pixel reset transistor threshold voltage shift. High electric field distribution at both sides of the transfer gate in a 4T pixel is responsible for the degradation as well. As for the future radiation tolerant CIS design, the p-well guarded structure to suppress the leakage path formation after radiation damage will be implemented.

Acknowledgements

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Reference

[1] M. Cohen and J. P. David, "Radiation-induced dark current in CMOS Active Pixel Sensors," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2485-2491, Dec. 2000.

[2] D. A. Neamen, Semiconductor physics and devices, 3rd ed, pp. 465-500, McGraw Hill, 2003

[3] X. Wang, P. R. Rao and A. J. P. Theuwissen, "Fixed-pattern noise induced by transimission gate in pinned 4T CMOS image sensor pixels," *ESSDERC 2007-Proceedings of the 37th European Solid-State Device Research Conference* , art. no. 4430955, pp. 370-373, 2007

[4] J. Tan, A. Baiano, R. Ishihara, C. I. M. Beenakker, "2D simulation of hot-carrier induced degradation and reliability analysis for single grain Si TFTs," *The annual workshop on semiconductor advances for future electronics and sensors*, pp. 600-603, 2008.

[5] Sentaurus device user guide, 2006

[6] V. Goiffon, et al., "Ionizing Radiation Effects on CMOS imagers manufactured in deep submicron process," *Proceedings of SPIE - The International Society for Optical Engineering*, 6816, art. no. 681607.