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High-Performance (S. S. < 100 mV/dec) Poly-Si TFTs with Laser Annealed Channel and High-κ Metal-Gate on Glass Substrate

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Abstract

We demonstrate high performance LTPS-TFTs with a TaN/Hf-based gate-stack and channel film by laser-annealed on glass (Glass-Substrate High-k Metal-gate TFTs, called GSHM-TFTs). The GSHM-NTFTs exhibit a very low threshold voltage, steep subthreshold swing S.S.~ 95mV/dec. and high I_{ON}/I_{OFF} ratio>10^7. On the other hand, P-TFTs exhibit subthreshold swing S.S.~ 154 mV/dec. and I_{ON}/I_{OFF} ratio even higher than 10^8 without any hydrogen- related plasma treatments. Additionally, the impact of grain boundaries in poly-Si is also investigated.

Introduction

High-performance low-temperature poly-Si thin film transistors (LTPS-TFTs) are recently developed for the employment of active-matrix liquid crystal displays on a glass substrate and for driving integrated circuits for the application of system-on-panel (SOP) and the three-dimensional (3-D) circuit integration elements such as SRAMs and DRAMs [1]–[3]. Besides, high-speed display driving circuits require thin film transistor (TFTs) to operate at low voltages and high driving currents, with a low threshold voltage. However, the grain boundaries in poly-Si channel film degrade the subthreshold swing S.S., threshold voltage V_{TH}, and field-effect mobility μ_{FE} and result in a large operation voltage [4]–[5]. Some high-κ materials, including Al_2O_3, Ta_2O_5, and HfO_2, were proposed to preserve the physical dielectric thickness while increasing the gate capacitance [6]–[8]. In this work, we demonstrate LTPS-TFT with TaN gate, HfO_2 gate dielectric on laser-annealed poly-Si channel film for the n-channel and p-channel, respectively. High-performance LTPS-TFTs of a lower threshold voltage, excellent S.S., and high μ_{FE} for NTFTs and PTFTs can be obtained, which are very promising for the realization of SOP and 3-D circuit integration.

Device Fabrication Process

Fig. 1 shows the process flow of the GSHM-TFTs in this work. First, the active region was defined on the laser-annealed poly-Si film. Then, 50-nm HfO_2 dielectric was deposited by atomic-layer chemical-vapor-deposition (AIXTRON Tricent) system at a substrate temperature of 500℃. 300-nm TaN gate was deposited by sputter at room temperature (Fig. 1(a)) and patterned by reactive ion etching (Fig. 1(b)). After the gate-stack formation, source and drain (S/D) regions were implanted with phosphorus and BF_2, then activated at 600℃ for 24-h annealing in a N_2 ambient (Fig. 1(c)). Finally, metallization and sintering were performed to complete the fabrication (Fig. 1(d)). After fabrication process, NTFTs devices underwent another 10 min NH_3 plasma treatment for passivation. Additionally, the impact of grain boundaries in poly-Si has been experimentally investigated by adapting AC and DC measurement.

Results and Discussion

A. Transistor Performance and Characteristics:

Fig. 2 shows the I_D-V_G characteristics of GSHM-NTFTs and Control-TFTs, respectively. The GSHM-NTFTs exhibit excellent swing ~95 mv/dec and high μ_{FE}~112 cm^2/V.s which is better than those of Control-TFTs with 30-min plasma treatment (S.S.~450 mV/dec.; low mobility). This improvement can be attributed to the larger poly-Si grain formed by the laser annealing process and the high gate-capacitance with HfO_2 gate dielectric. Fig. 3 shows the well-behaved I_D-V_G characteristics for the GSHM-PTFTs (SS~154mV/dec. and V_{TH}~ 0.063V, I_{OFF}~10^{-13}A). The supply voltage can be lowered down to 2V/3V (N/P) with a high I_{ON}/I_{OFF} ratio>$10^7/10^8$ (N/P). In the Fig.4, we show the ID-VG characteristics of NTFTs and PTFTs before NH_3 plasma treatment, respectively. We can observe that the PTFTs exhibit a better performance than NTFTs. In LTPS TFTs, trap states in the grain boundaries and at the poly-Si/SiO_2 interface are more than MOSFETs. In inversion conditions, electron and hole concentrations distribution are different [9]. The electrons concentrations peak is near interface that results in the poorer S.S. due to more scattering. Besides, the higher I_{OFF} may be due to the junction leakage of drain side caused by process damage. Additionally, these devices exhibit extremely high drive currents and high field-effect mobility μ_{FE} (112 cm^2/V-s for n/ 86 cm^2/V-s for p), as illustrated in Fig. 5 and Fig. 6, respectively. The high driving current would be very suitable for the application of SOP and 3-D circuit integration. TABLE I compares device performance between this work and published high performance TFTs data.

B. Impact of Grain Boundaries in Poly-Si:

In the Fig. 7, pulse I-V curves [10], with 100 ns pulse width, were used to measure GSHM-TFTs and compared to DC I-V curves. Pulse I-V measurement technique has been reported that the charge effect of high-k dielectrics is negligible, which results in an increase of the measured driving current compared to the DC technique for MOSFETs [11]. However, in TFTs, the DC I-V curves exhibit better characteristics, as shown in Fig. 7. The reason may be due to the randomly oriented grain boundaries (GBs) exist in the channel of TFTs, mixing the longitudinal and latitudinal orientations. The grain boundaries in the channel of TFTs results in a longer transient time to form an inversion layer and a higher V_{TH} [12]. As using the pulse I-V measurement technique with 100 ns pulse width, the pulse width is very short and not enough to form the inversion formation. Therefore, the on current of the pulse I-V curves is less than that of the DC I-V curves.

Conclusions

The combination of high-κ gate dielectric and laser-annealed poly-Si channel film for LPTS-TFTs has been proposed. The N and P GSHM-TFTs can achieve a high μ_{FE}, low V_{TH}, and excellent S.S. simultaneously. This combination of TaN/HfO_2 gate stack structure and laser-annealed poly-Si channel would be very promising for the application of SOP. Additionally, the grain boundary in poly-Si result in the on current of the pulse I-V curves is less than that of the DC I-V curves.

References

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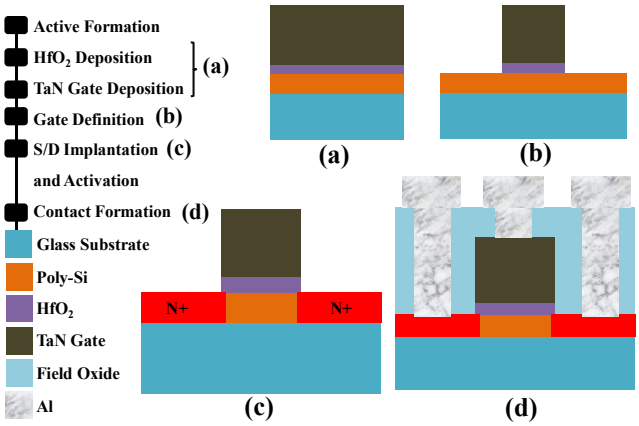

Fig. 1. Process flows of GSHM-TFTs in this work.

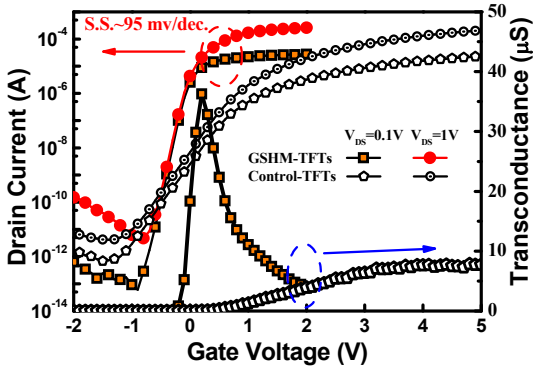

Fig 2. The I_D-V_G characteristics of GSHM-NTFTs and Control-TFTs, respectively. The GHSM-NTFT exhibits a excellent I_D-V_G characteristics.

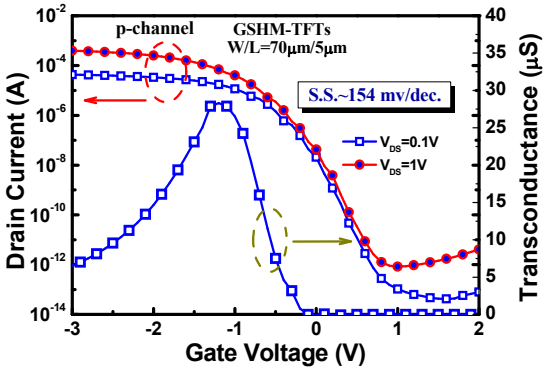

Fig 3. The I_D-V_G characteristics of GSHM-TFTs with p-channel. The well-behaved I_D-V_G characteristics for the GSHM-PTFTs was showed.

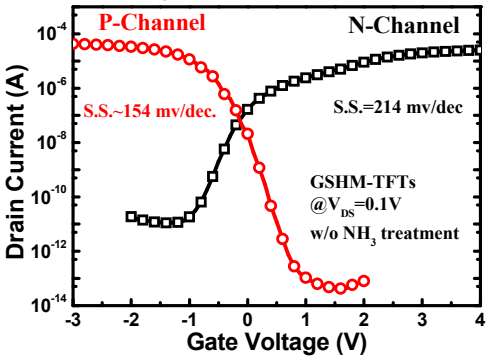

Fig 4. The I_D-V_G characteristics of GSHM-N/P TFTs before NH_3 plasma treatment, respectively.

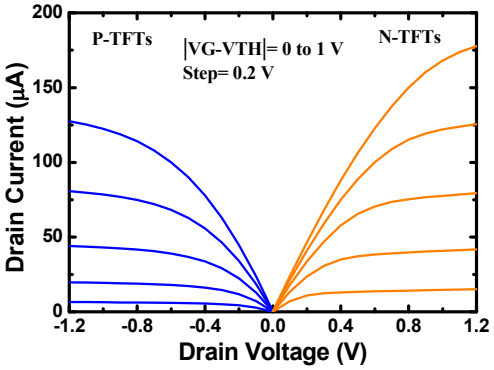

Fig 5. The output characteristics of GSHM-TFTs with n-channel and p-channel, respectively. The high driving current was achieved at $|V_{DS}|$=1.2V.

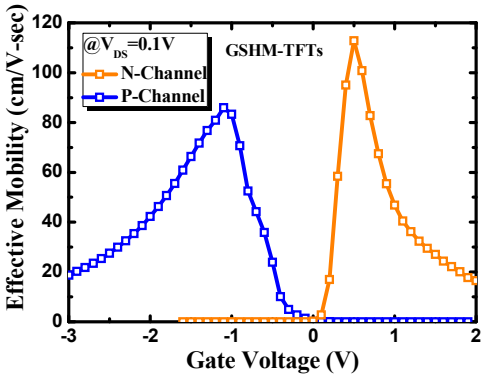

Fig 6. The high effective mobility of GSHM-TFTs with n-channel and p-channel, respectively.

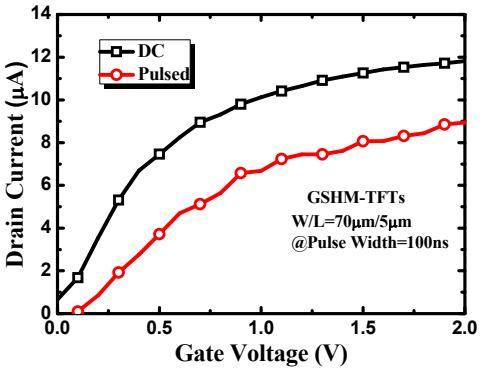

Fig 7. The I_D-V_G characteristics of GSHM-NTFTs with DC and Pulsed measurements, respectively. In TFTs, the DC I-V curves exhibit better characteristics

	This Work		Ref. A	Ref. B	Ref. C		Ref. D
	NTFTs	PTFTs	NTFTs	NTFTs	NTFTs	PTFTs	PTFTs
Channel	LASER Annealed		SPC	SPC	MILC		SPC
Gate Stack	TaN / HfO_2		TaN / $HfSiO_X$	Poly-Si/ HfO_2	Poly-Si / SiO_2		Poly-Si/ $HfSiO_X$
W/L (μm/μm)	70/5		150/0.3	0.1/1	10/5		5/10
VTH (V)	-0.3	0.063	0.75	0.3	3.8	-5.7	-0.91
EOT (nm)	14		2.8	2.7	100	100	25.5
μ_{FE} (cm2/V-s)	112	86	33	39	70	98	27.45
I_{ON}/I_{OFF} (V_{DD})	$>10^7$ (1V)	$>10^8$ (-1V)	$>10^6$ (1V)	$9.7x10^6$ (1V)	$1.4x10^7$ (5V)	$3.4x10^7$ (-5V)	$4.12x10^6$ (-2V)

Table 1. Comparison of important parameters from this work to other published results. [A] M. H. Lee et al. SSDM, pp1036-1037,2009. [B] C.-P. Lin et al., EDL, vol. 27, no. 5, pp. 360–363, May 2006. [C] Z. Meng et al. ED, vol. 47, no. 2, pp. 404–409, 2000. [D] M.-J. Yang, et al., EDL, vol. 28, p. 902, 2007.