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Electron and hole mobility comparison in a single Ge-MOSFET fabricated on 50 nm-thick GeOI substrate

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1. Introduction

Germanium (Ge) has attracted much attention for "beyond Si-CMOS device" from the viewpoint of its higher mobility than Si. In particular, Ge p-MOSFET shows quite a high mobility over Si. Recently we demonstrated very high electron mobility (~1500 cm^2/Vsec) in Ge n-MOSFET as well [1]. However, critical factors determining the carrier mobility in Ge MOSFETs are still unclear, because it is difficult to compare electron mobility with hole one directly in the same MOSFET.

We have paid attention to the fact that the difference between inversion and accumulation in ultra-thin Ge channel case is not an issue for discussing the carrier transport because the confinement potential is formed not electrically but by the geometrical boundaries. In this paper, we show a direct comparison of electron mobility with hole one in a single MOSFET fabricated on 50 nm-thick low-doped GeOI.

2. Device fabrication

50 nm-thick GeOI was prepared by careful wet etching process from lightly n-doped 100 nm thick-GeOI wafer. Buried SiO_2 thickness was about 400 nm, which was determined by spectroscopic ellipsometry. First, the mesa type Ge island was defined by wet etching as shown in **Fig. 1**. Al was employed for metal source/drain for simplicity. Ge/Al contact at source and drain should show Schottky characteristics but a large contact area enabled us to measure both n-channel and p-channel FETs. Large MOSFETs with L=330, 430 μm and W=130 μm were made. The device structure investigated is schematically shown in **Fig. 2**. In addition, the double mask length (*double Lm*) method [2] was used to accurately subtract the series resistance for determining the intrinsic carrier mobility.

3. Results and Discussion

The output characteristics in bottom gated p-channel MOSFET is shown in **Fig. 3**. Metal source/drain p-channel FET operates quite well. It is worthy of mentioning that the capacitance measured includes the capacitance between substrate and metal contact. By using *double* L_m method, such parasitic capacitances can be automatically removed and only the channel capacitance can be obtained. However, since the present device showed ambipolar behavior, channel capacitance was hard to estimate. Therefore, although in the accurate *double* L_m method,

$$\mu_{eff} = (L_{m,1} - L_{m,2})^2 \cdot \frac{1}{\int (C_{GC,1} - C_{GC,2})} \cdot \frac{1}{V_{DS}} \cdot \left(\frac{1}{I_{DS,1}} - \frac{1}{I_{DS,2}} \right)^{-1}$$

should be used for mobility extraction, $LW \cdot C_{ox}(V_G - V_{TH})$ was used for the channel carrier estimation. Thus, *double* L_m method is modified to

$$\mu_{eff} = \frac{L_{m,1} - L_{m,2}}{W_{eff}} \cdot \frac{1}{C_{OX}(V_G - V_{TH})} \cdot \frac{1}{V_{DS}} \cdot \left(\frac{1}{I_{DS,1}} - \frac{1}{I_{DS,2}} \right)^{-1}$$

Fig. 4 shows both electron and hole mobility in a single MOSFET fabricated on 50 nm-thick GeOI. There are many reports that electron mobility is degraded while hole mobility is remarkable in Si-inserted Ge MOSFETs [3]. The result clearly shows that the interface between Ge and SiO_2 affects differently on electron channel and hole channel. Thus, the Si-passivated Ge interface cannot be used for n-channel FET in case that Si is subject to oxidation. The same kind of mobility comparison was performed on SOI and GeOI [4] using pseudo-MOSFET technique. But it includes the large series resistance effect intrinsically.

The reason why Ge/SiO_2 interface is different from Si/SiO_2 one for the electron channel is still unclear, but we can conclude that there are so many scattering centers for electron channel at the same interface. In fact, by lowering the measurement temperature, the mobility is degraded. This fact implies much more coulombic centers at the Ge/SiO_2 interface. The recent high electron mobility was achieved in Ge/GeO_2 gate stack, where the interface states are dramatically reduced.

4. Summary and Future Outlook

We evaluated electron and hole mobility in a single MOSFET fabricated on GeOI substrate. The channel in 50 nm-thick Ge is fully depleted and the interface is Ge/SiO_2 for both electron and hole channels. By using the modified *double* L_m method, electron mobility was compared with hole one directly on the same MOSFET. It was clearly found that electron mobility was degraded compared with hole one in case that the electron channel interface was SiO_2. This is quite

different from the results on SOI. Si/SiO_2 interface is advantageous both for electron and hole, while Ge/SiO_2 is not appropriate for electron channel. In ultra-thin GeOI MOSFETs, the majority carrier operation on high-doped Ge will be possible like junction-less transistor [5], and the preliminary results on low-doped Ge are shown in **Fig. 5**, where the substrate type is turned by the bottom gate while the top gate controls the channel. There will be many other device options using both inversion and accumulation modes on thin GOI in addition to utilizing the Fermi-level pinning at metal/Ge.

Acknowledgements

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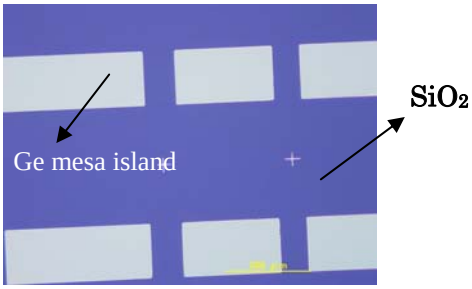

Fig. 1. Microscopic image of Ge mesa island on SiO_2.

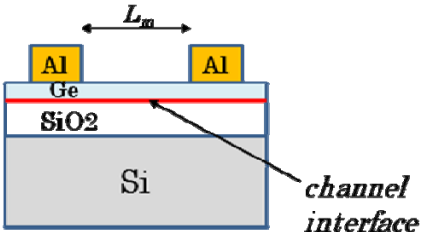

Fig. 2. Schematic of devices structure on GeOI. Ge thickness is 50 nm, so both inversion and accumulation channels are working. BOX thickness is 400 nm.

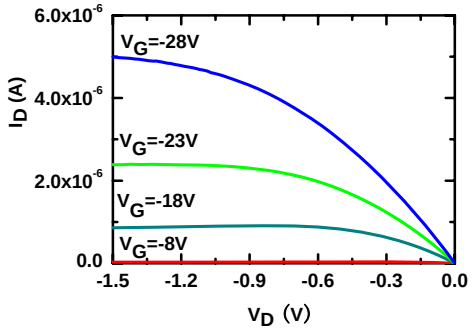

Fig. 3. Bottom gated p-channel FET. BOX SiO_2 works as gate insulator. Hole inversion layer is formed.

References

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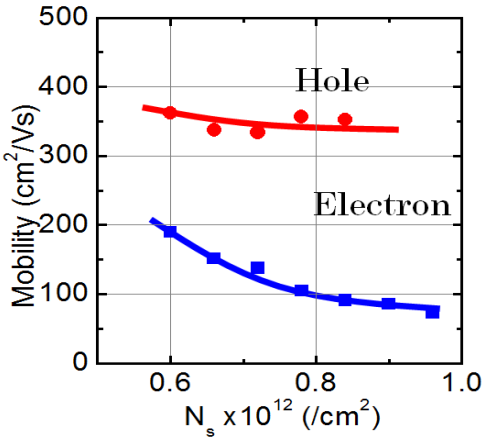

Fig. 4. Mobility comparison between electron and hole in 50 nm-thick GeOI channel. Electron mobility is significantly degraded compared with hole one.

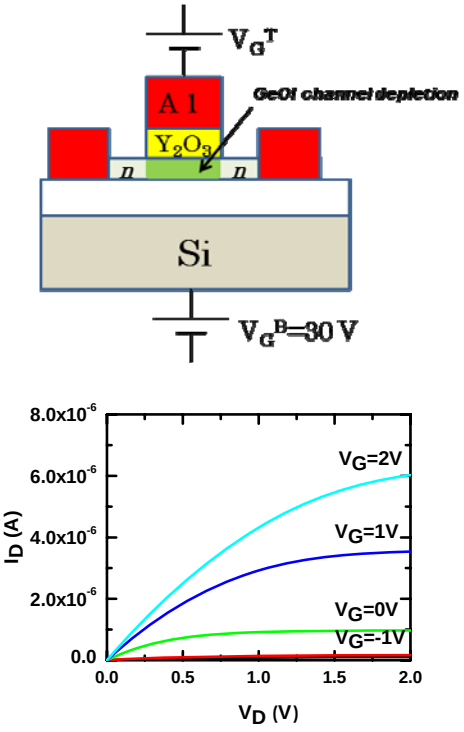

Fig. 5. Top-gated n-MOSFET on GeOI. The depletion type MOSFET will be possible for ultra-thin GeOI operation. The gate insultor is 30 nm-thick Y_2O_3. The bottom gate bias is 30 V to form n$^-$extension layer. It is not optimized yet, so the series resistance is quite high.