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Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16-nm CMOS Devices

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1. Introduction

CMOS device with metal gate is one of key technologies for improvement of device performance and the reduction of intrinsic parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of nanosized metal grains [1-3]. In this work, we for the first time estimate the impact of the metal gate work-function fluctuations (WKF) using experimentally calibrated full 3D device simulation on high-κ/metal gate technology [4,5]. The fluctuations of the threshold voltage (V_{th}) and gate capacitance (C_G) are investigated. The WKF induced V_{th} fluctuation (σV_{th}) based on our 3D simulation are 36.7 mV and 42.5 mV for NMOS and PMOS, which are rather different from the result of averaged work-function method [1] due to localized random work-function effect. In addition, the number and position effect of different grain orientation are analyzed and discussed.

2. Methodology and Results Discussion

The control NMOS devices we investigated are the 16-nm-gate bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfO_2 gate stacks of 4.52eV effective work-function and an EOT of 0.8 nm. For PMOS, we use Al incorporation to tune the work-function of TiN [6], and the control PMOS device's effective work-function used here is 4.76eV. Due to the work-function is tuned by the dipole formation of HfO_2/SiO_2 interface; the Al incorporation will give a fixed offset of work-function, as in Fig. 1(a). Figure 1(a) also shows the work-function fluctuation (WKF) sources, metal material properties, and the validated performance of the devices according to ITRS roadmap for low operating power [4]. To describe the WKF induced characteristic fluctuations, in contrast to averaged work-function (AWF) method or compact model [1,2], we directly partition the device gate metal material into many sub-regions according to the grain size [3], and then we randomly generate the work-function to each sub-region according to the material properties and map them into device gate for our experimentally calibrated three dimensional (3D) quantum-corrected device simulation [4], as shown in Fig. 1(b). Two hundred statistically random devices are generated to examine the WKF induced threshold voltage (V_{th}) and gate capacitance (C_G) fluctuations.

Figure 2 shows the I_D-V_G curves induced by WKF of NMOS and PMOS, where the control devices with effective work-function 4.52eV and 4.76eV are the red thick symbol curves, and threshold voltage fluctuation (σV_{th}), the normalized on- and off-current fluctuations (σI_{ON} and σI_{OFF}) are shown in the inset. Their values are 36.7 mV, 5%, 57%, 42.5 mV, 10%, 46%, respectively. Figure 3 compares σV_{th} between AWF method [1] and our 3D device simulation, the AWF method significantly underestimated the WKF induced σV_{th}. To further understanding the physical mechanism of WKF induced device characteristic fluctuations; we investigate the on-state potential and charge distribution at channel surface from one of WKF devices. Due to the probabilistic distribution of work-function, the effective work functions of two-hundred devices are not a deterministic value and results in device to device performance variation. Figure 4(a) shows the large-scale statistically computed results of V_{th} as a function of the number of TiN <200> (higher work-function) contained for NMOS. From the grain orientation with high work-function point of view, the effective work-function of a single device increases as the number of TiN <200> increases, result in a higher V_{th}. Moreover, it is found that even for devices with the same numbers of TiN <200> inside the gate, the effect of nanoscale grain orientation position induces different fluctuations of characteristics in spite of there being the same number of TiN <200>. To explore the grain orientation-position-induced V_{th} fluctuation, the on-state (V_G = 0.8 V, V_D = 0.8 V) potential distributions with containing nine TiN <200> but different position inside the gate are investigated, as shown in Figs. 4(b) and (c). The potential distributions are 1 nm below the channel surface. For a device with TiN <200> located at the middle of channel, the corresponding potential distributions are significant decreased in these areas, which significantly changes the electron conducting path and induce larger V_{th}. Figure 4(d) presents the charge distribution of the channel surface extracted from Fig. 4(b) at V_G = 0.8 V and V_D = 0 V. We can clearly find the charge distribution is strongly governed by different local work-function of gate metal orientations, and such phenomenon can not be predicted by AWF methods. Comparison between the two methods implies that the AWF uses an effective work function for each device to calculate the performance, which assumes a uniform inversion charge density at the channel surface. The difference between these two methods can be considered in terms of the band diagram, which leads to different substrate band bending and varying throughout the channel. Figure 4(a) shows the C_G-V_G curves with WKF for NMOS, and Fig. 4(b) summarized C_G fluctuations (σC_G) at different gate bias. The results show that WKF induced largest σC_G at moderate inversion region. Due to the screen effect of accumulation or inversion layer, the WKF brought less impact on σC_G at these bias conditions.

3. Conclusions

In this work, we have examined the WKF using full 3D device simulation on high-κ/metal gate technology. This approach considers the effect of local crystal orientation of nanosized metal grain which is quite different from the recent reported averaged work-function method [1]. The WKF induced σV_{th} and σC_G of COMS devices are studied with respect to local work-functions resulted from different number and position of metal grain orientation, which may induce significant performance degradation and uncertainty of circuits and systems.

Acknowledgement

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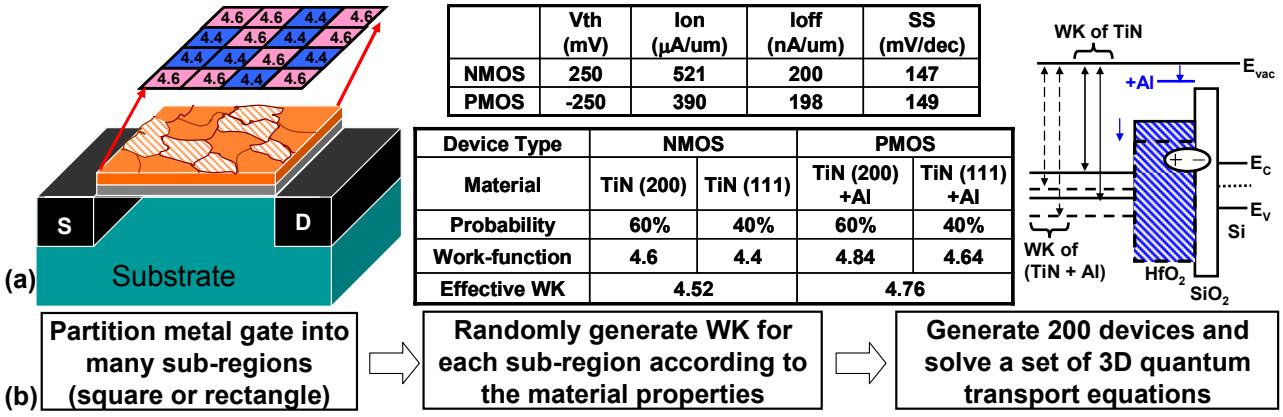

	Vth (mV)	Ion (μA/um)	Ioff (nA/um)	SS (mV/dec)
NMOS	250	521	200	147
PMOS	-250	390	198	149

Device Type	NMOS		PMOS	
Material	TiN (200)	TiN (111)	TiN (200) +Al	TiN (111) +Al
Probability	60%	40%	60%	40%
Work-function	4.6	4.4	4.84	4.64
Effective WK	4.52		4.76	

Figure 1. (a) The source of random variation, performance of devices, and metal properties used in this work. The PMOS gate materials with Al incorporation gives a fixed work-function offset for different orientation. (b) The simulation flow chart to describe the WKF induced characteristic fluctuations, we directly separate the device gate metal material into many sub-regions, and then we randomly generate the work-function to each sub-region according to the material properties and map into the device gate for 3D device simulation.

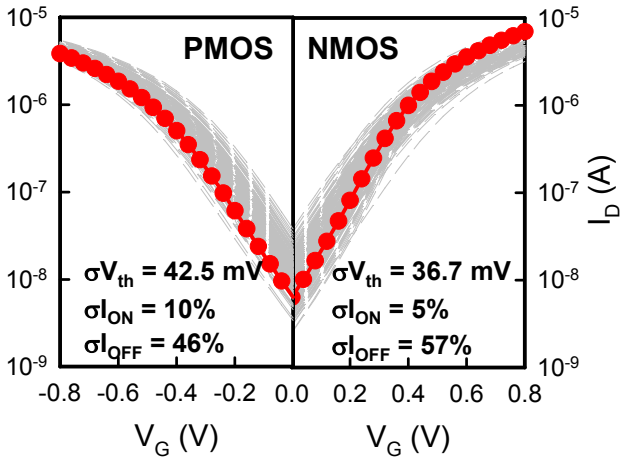

Figure 2. The WK fluctuated I_D-V_G curves for the tested (a) NMOS (b) and PMOS devices, where the nominal curves with WK of 4.52 eV and 4.76 eV are the red thick symbol lines. The σV_{th}, and the normalized σI_{ON} and σI_{OFF} are listed in the inset.

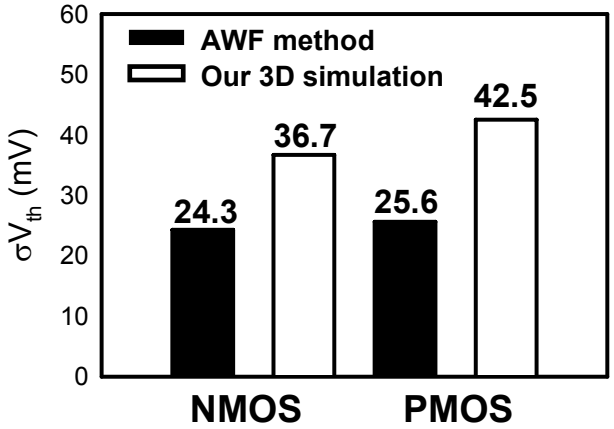

Fig. 3. σV_{th} comparison between AWF method and our 3D device simulation. AWF method underestimates WKF because it does not reflect the nonuniform surface charge distribution due to the different crystal orientation of nanosized metal grain locally.

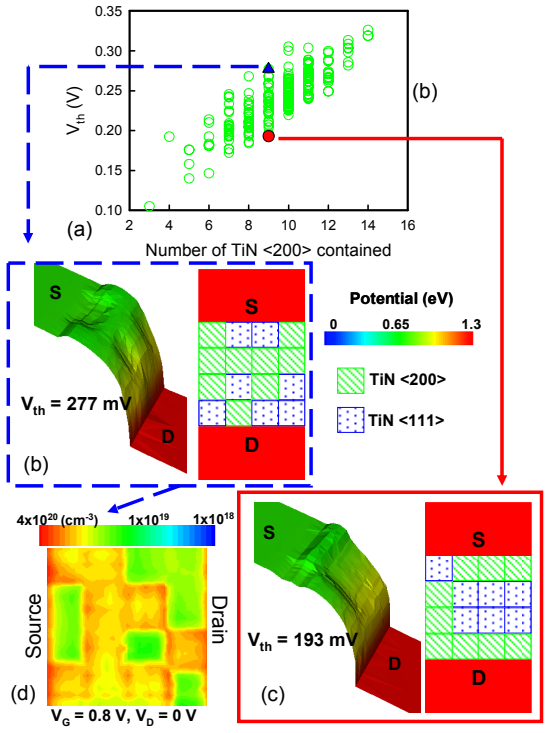

Fig. 4. (a) Threshold voltage distribution as a function of number of TiN <200> contained for NMOS. The on-state (V_G = 0.8 V, V_D = 0.8 V) potential distributions of (b) higher V_{th} and (c) lower V_{th}, devices with the same number of TiN <200>. (d) The charge distribution extracted from (b) at V_G = 0.8 V, V_D = 0 V.

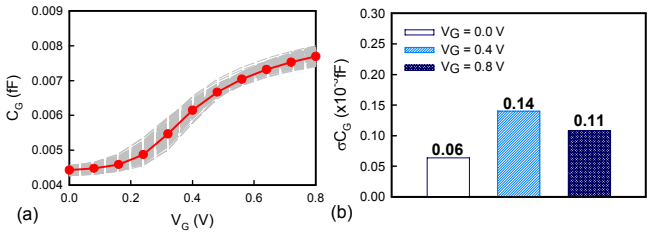

Fig. 5. (a) The WK fluctuated C_G-V_G curves of NMOS. (b) The summarized σC_G of device at different gate bias.