Technology Computer Aided Design of 65nm SOI MOSFETs through Integrated Process and Device Simulations

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Abstract—Integrated process and device simulations were used to predict sub-65nm SOI device performance. Physically-based process models, generalized from Si to SOI, describe dopant implantation and diffusion, including amorphization, defect interactions and evolution, as well as dopant-defect interactions. The models are used within a unique simulation tool to reproduce the electrical characteristics of SOI devices.

1. Introduction

Ion implantation, diffusion, and thermal annealing are crucial steps in the simulation of silicon processing since they induce significant fluctuations in the electrical characteristics of advanced MOS transistors.

Recently, SOI structures have stood as a possible candidate to fulfil the requirements defined in the ITRS [1]. Indeed, reduced short channel effects, improved speed and reduced power consumption can all be obtained in CMOS devices based on SOI [2].

In this work, a process simulation set-up based on the State-of-Art diffusion and activation models of dopants is used. More specifically, the recently developed model [3] investigating the influence of the Silicon/Buried Oxide (Si/BOX) interface on interstitial point defect evolution and dopant diffusion is applied to a standard 65nm CMOS process by means of TCAD simulations. The application to 65nm SOI MOSFET devices demonstrate that our physically-based models not only can generate accurate defect evolution and dopant diffusion profiles for present advanced CMOS process, but can also obtain remarkable prediction of device characteristics such as SOI CMOS devices. This can provide important insight for optimizing the device performance in TCAD simulations for manufacturing.

2. Implantation and diffusion models

In this work, several improved diffusion simulation models developed in the EC project ATOMICS and implemented in the commercial software Sentaurus Process [4] were used. As-implanted interstitial and vacancy profiles are generated using the Monte Carlo model with cumulative damage. The dopant diffusion is described by a 5-stream drift-diffusion model [4-5] dopant precipitation is considered when the solid solubility limit is reached. The complete defect evolution model [6] is based on the Ostwald ripening mechanism [7], with the surface being a very efficient sink for silicon interstitials. These phenomena drive the point defect supersaturation, acting on dopant transient enhanced diffusion (TED) and boron-interstitial [8] or arsenic-vacancy [9] clustering behavior. Regarding SOI materials, we have studied [10] the mechanisms contributing to the evolution of point defects in

SOI substrats, i.e. the enhanced End Of Range (EOR) defects dissolution due to the presence of the Si/BOX interface. Based on these experiments, existing models for the simulation of TED in silicon have been modified to include an additional buried recombination site for interstitials.

2. Process simulation results

The simulated PD-SOI CMOS devices are manufactured using a 70nm Si layer thickness. The gate stack is made using a 20Å thermal nitrided oxide and thick poly-silicon. Next, gates are patterned down to L_G=50nm. TEM picture and simulated 65nm PD-SOI PMOS are compared in Fig. 1.
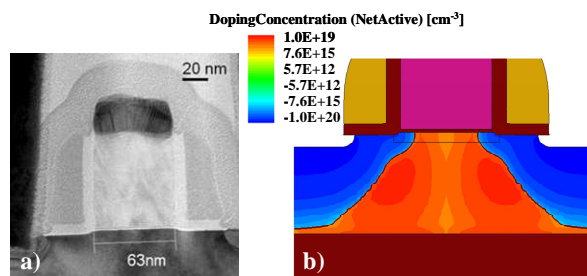

Fig. 1: Cross-sectional TEM showing poly=63nm (a) and simulated 65nm PD-SOI PMOS (b).

During the annealing step, evolution and distribution of extended defects can be monitored in order to better understand the dopant diffusion acceleration due to point defect created by the implantation step. Indeed, applied to this standard process of the 65nm SOI device, the model usefulness [3] is demonstrated in Fig. 2.
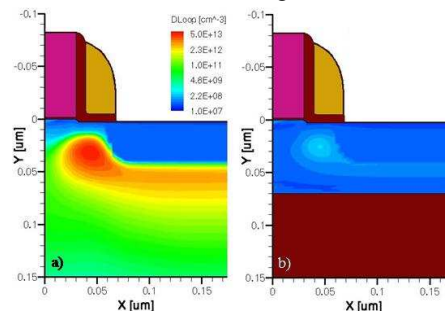

Fig. 2: 2D simulation of defects densities at the end of the process flow showing the effect of the model for point defects recombination at the Si/BOX interface.

At the end of the same implantation/diffusion process flow, the dissolution of EOR defects is almost completed in the SOI devices (Fig. 2b) but not in the standard Bulk Si (Fig. 2a). Moreover, as we can observe in Fig. 2, the spatial distribution of dislocation loops is not uniform and the defects dissolution

is influenced by the presence of the additional interface Si/BOX acting as a perfect sink of point defects.

The shape of the different active zone regions of the simulated bulk Si and PD–SOI PMOS with a gate length of 65nm is presented in Fig. 3. It shows that the boron S/D junction length (T_{Si}) decreases when passing form bulk Si (Fig. 3a) to SOI (Fig. 3b). The boron diffusion profile in the SOI structure is shallower than the one in the bulk Si (Fig. 3). Indeed, in bulk Si, the boron diffusion profile is controlled by interstitial supersaturation due to the Oswald Ripening mechanism of implantation induced extended defects. In the SOI structure, with the additional interface acting as a sink of excess point defects, EOR defects dissolution is faster, leading to minimized TED of dopants. Thus, boron diffusion in SOI is reduced compared to bulk Si. Comparable results are achieved for phosphorus which diffuses mainly by the interstitialcy mechanism.
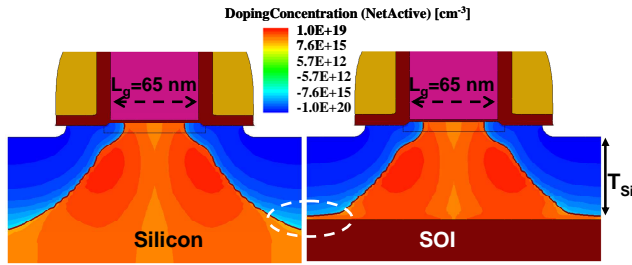

Fig. 3: Simulated net doping profile for a 65nm gate length standard PMOS. a) bulk Si and b) PD-SOI.

4. Device simulation and discussion

Device simulations were done using Sentaurus Device [4]. A gate voltage Vg of 1.2V was applied to the gate electrode, while a drain voltage Vd of 0.05V was applied for the low-field and Vd=1.2V for the high-field case.
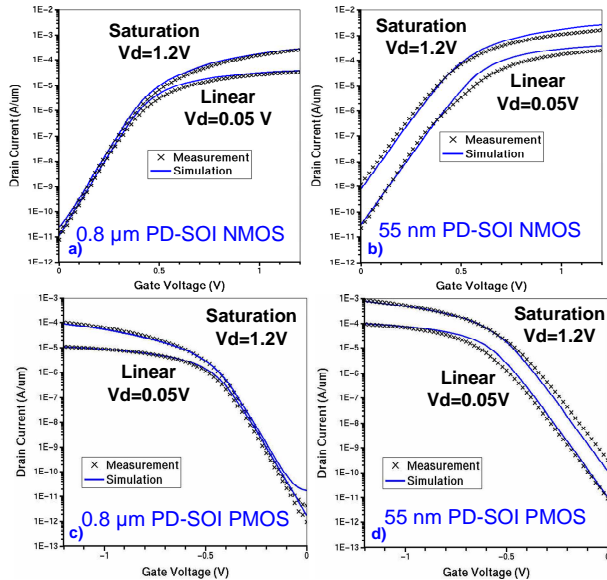

Fig. **4**: Drain-current versus gate voltage characteristic of a 0.8µm (a) and 55nm (b) PD-SOI NMOS and 0.8µm (c) and 55nm (d) PD-SOI PMOS devices. (Symbols: Measurement, Lines: Simulation).

PD–SOI Id-Vg with various gate lengths (L_G) ranging from

50nm to 10µm are simulated and resulting electrical currents (L_G=55nm and L_G=800nm for instance) are shown in Fig. 4.

The experimental measurements of the same electrical characteristics are also reported. First, excellent prediction of Id–Vg curves is obtained using our TCAD simulation, demonstrating the accuracy of our process simulation set-up.

The short channel effect extracted from PD–SOI NMOS and PMOS devices is also investigated. Fig. 5a/c depict the variations of the threshold voltage (V_{th}) roll-off, and Fig. 5b/d the drain-induced-barrier lowering (DIBL) characteristics as a function of the gate length and compared to experimental data. The Vth roll-off characteristic of a pocket effect is well reproduced by the simulation. It is clear that the 2D doping profiles obtained from our process simulations can simulate device characteristics upon transfer to a device simulator.
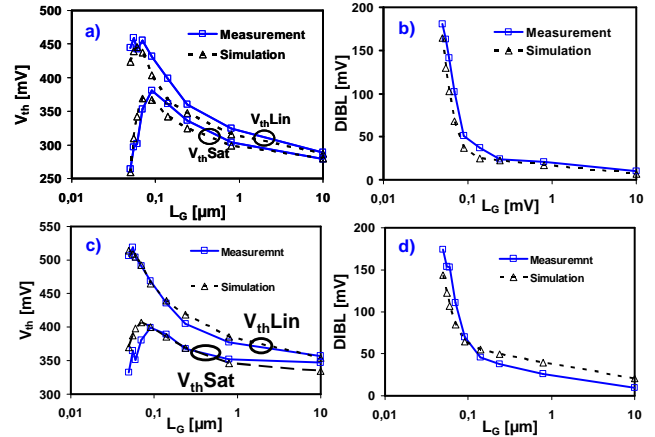

Fig. 5: Comparison between experimental and simulated V_{th} roll-off characteristics (a-c) and DIBL (b-d) of PD-SOI NOMS and PMOS devices. V_{th} roll-off characteristics have been measured for V_{th}Lin, Vd=0.05V and V_{th}Sat, Vd=1.2V.

5. Conclusions

Integrated process and device simulations were used to predict sub-65nm SOI device performance. Physically-based models were used to simulate accurately both implantation defect evolution and dopant diffusion in the SOI substrats. The obtained 2D doping profiles correctly predict the short-channel behavior of devices and illustrate the necessity of physically-accurate process models for the optimization of aggressively-scaled SOI devices.

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