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The Observation of the Random Dopant Fluctuation in Strained-SOI Devices

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Abstract- In this paper, the device performance and V_{th} variation of the MOS devices on the SOI and strained-SOI (SSOI) have been examined. Both the effects of operation mode and temperature on V_{th} variation have been examined for SOI and SSOI nMOSFETs. It was characterized by the parameter, B_{VT}, an indicator of V_{th} variation. Experimental verifications on nMOSFETs for both technologies with tensile-stress enhancement have been made. For SSOIs, it shows the expected drain current enhancement and smaller B_{VT} than that of SOIs. Furthermore, SSOIs exhibit a weak dependence of V_{th} variation on the drain bias as a result of the strain effect in the device which makes it successful for good short channel effect (SCE) immunity.

1. Introduction

As CMOS devices are scaled to the nanoscale dimension, reducing V_{th} variation becomes a significant issue for advanced CMOS technology. Recent studies [1,2] have revealed that random dopant fluctuation (RDF) is the major source of V_{th} variation in scaled bulk CMOS. To improve the RDF, FDSOI or FinFET with undoped (lighter) channel [3-5], has been proposed to reduce the variability effectively. However, so far, none has been reported on the variability of SSOI devices. As a consequence, we are interested in understanding the variability of SSOI devices.

In this paper, the drain current enhancement of SOIs and SSOIs will be first examined. Then, the variability study based on the V_{th} variation and the effect caused by the device operation mode, self-heating effect, and the drain bias will be presented. The basis of the V_{th} variation is analyzed using the Takeuchi plot [6], i.e.,

$$\sigma V_{th} = B_{VT} \sqrt{T_{inv}(V_{th} + V_O)/LW} \qquad (1)$$

along with a set of formulations in Table 1.

2. Device Preparation

SSOI device, (no Ge incorporation), as shown in Fig. 1, was built on a thin (70nm) top silicon film isolated from the substrate by buried oxide (145nm) with UMC 65nm SSDOI technology, and at the same time, biaxial tensile strain in the thin film is formed.[7] Moreover, for performance enhancement, CESLs are used to provide uniaxial tensile strain. The device has 14Å (physical thickness) SION gate oxide. The control SOI and conventioal bulk devices were also made for comparison. Devices with various areas were measured for Takeuchi plots. The device threshold voltage was measured by the $g_{m(max)}$ and the constant current method.

3. DC Performance of SOI and SSOI nMOSFETs

Fig. 2 shows an average improvement of 22% in drain current for SSOIs from long to short channel devices. Furthermore, Fig. 3 shows the I_{on}-I_{off} results for both SSOIs and SOIs. It indicates SSOIs gain more than ~12.5% over SOIs. Finally, $I_{DS}V_{GS}$-on and off curves are measured in Fig 4. In the linear region (V_{DS}=0.05V), currents in SSOI are smaller than SOI devices, while, in the saturation region (V_{DS}=1V), SSOIs are enhanced much more than SOI ones.

4. Factors Affecting the V_{th} Variation

Effect of the Operation Mode- Three operation modes, as summarized in Table 2, have been employed to observe the V_{th} variations of SOIs and SSOIs. Figs. 5 and 6 show the Takeuchi plots of SOIs and SSOIs, respectively. Fig. 7 shows the comparison of B_{VT} values for three different operation modes. The V_{th} variation among these three modes can be realized by localized body effect due to bulk bias variation along the channel. Mode A, with floating both body and substrate, results in a larger variation of V_{th}, since the source/drain junction is hard to control which then causes variation in the channel electric field distribution. Mode B is similar to the conventional bulk devices, but the SOI body doping concentration is low such that the parasitic resistance will make bulk voltage non-uniformly distributed. Since the doping concentration is better controlled, mode B shows less V_{th} variation than mode A. Mode C shows the best uniformity since the high substrate doping concentration make the substrate voltage uniformly coupled to the body, reducing localized body effect. Moreover, SSOIs have smaller B_{VT} in all operation modes as a result of the channel strain effect.

Effect of the Temperature- To understand the effect of temperature, devices are measured at elevated temperature (85^OC). It was found that B_{VT} is larger at 85^OC in Figs. 8(a)-(c). As the temperature increases, the thermal fluctuation of the lattice becomes larger. The carrier moving through the crystal is easier to be scattered by a vibration of the lattice. Therefore, the V_{th} variation is increased as the device is heated. Moreover, Fig. 8(d) shows that SOIs and SSOIs have smaller B_{VT}(%), derived in Table 1, which exhibit less impact on the temperature and a good suppression of the V_{th} Variation.

Effect of the Drain Bias-The effect of the drain bias(V_{DS}) on σV_{th} for SOIs and SSOIs was also examined. V_{th} was extracted by constant current method. Fig. 9 shows the result of weak dependence of σV_{th} on V_{DS} for SSOIs. V_{th} roll-off as a function of channel length is also shown that SSOIs have a better control on channel length in Fig. 10. These characteristics indicate good SCE immunity and small variability for SSOI devices.

In summary, SSOI device is useful in terms of current enhancement and lower RDF. Extensive comparisons between SSOI and SOI nMOSFETs have been justified on examining the device operating mode, self-heating effect, and the V_{th} roll-off. Results show better variability of SSOI devices with the strained channel. In particular, SSOI shows much better SCE immunity. These results provide a good understanding of the random dopant fluctuations of SOI devices with strained technologies.

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[1] F. Yang et al., *Symposium on VLSI Tech.*, p.208, 2007.
[2] T. Tsunomura et al., *Symposium on VLSI Tech.*, p.156, 2008.
[3] A. V-Y Thean, in *Tech. Dig. IEDM*, p.881, 2006.
[4] K. J. Kuhn, in *Tech. Dig. IEDM*, p.471, 2007.
[5] O. Weber et al., in *Tech. Dig. IEDM*, p.245, 2008.
[6] K. Takeuchi et al., in *Tech. Dig. IEDM*, p.467, 2007.
[7] K. Rim et al., in *Tech. Dig. IEDM*, p. 49, 2003.

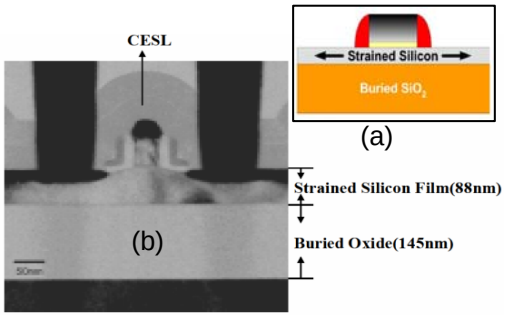


Fig. 1 (a) Schematic of the strained silicon on-insulator, (b) A TEM cross-sectional view of SSOI MOSFET.

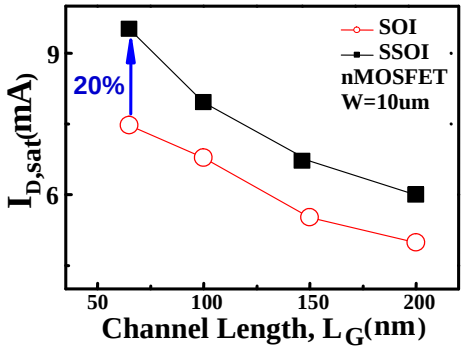


Fig. 2 Comparison of the $I_{D,sat}$ enhancements for nMOSFETs. SSOI devices show 22% current gain over control-SOI device.

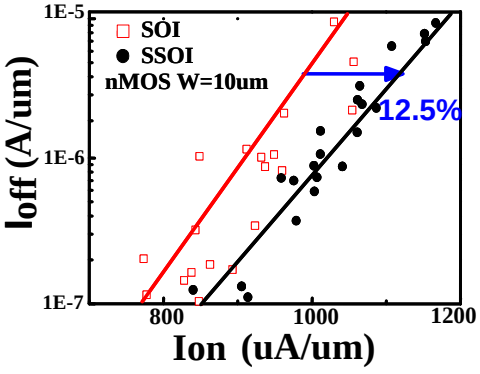


Fig. 3 Comparison of I_{on}-I_{off} between SSOI and SOI nMOSFETs. It shows that SSOI has a gain of 12.5% over that of SOI.

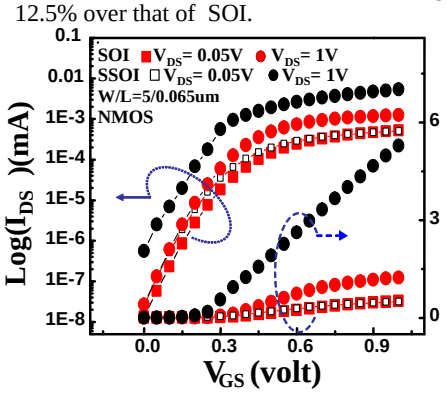


Fig. 4 Measured I_{DS}-V_{GS} at V_{DS}=1V and V_{DS}=0.05V for SOI and SSOI nMOSFETs.

$$\sigma V_{th} = \frac{q}{C_{inv}}\sqrt{\frac{N_{sub}W_{dep}}{3LW}},\ V_{th} = V_{FB} + \Phi_S + \frac{qN_{sub}W_{dep}}{C_{inv}}$$

$$= \frac{q}{C_{inv}}\sqrt{\frac{q(V_{th} - V_{FB} - \Phi_S)}{3LW}} = \sqrt{\frac{q}{3\varepsilon_{ox}}}\sqrt{\frac{T_{inv}(V_{th} - V_{FB} - \Phi_S)}{LW}}$$

$$= \sqrt{\frac{q}{3\varepsilon_{ox}}}\sqrt{\frac{T_{inv}(V_{th} + V_0)}{LW}} = B_{VT}\sqrt{\frac{T_{inv}(V_{th} + V_0)}{LW}} \quad -(1)$$

$$B_{VT}(\%) = \frac{B_{VT}(85^oC) - B_{VT}(25^oC)}{B_{VT}(25^oC)} \times 100\% \quad -(2)$$

Table 1 (1) Derivation of the correlation between σ V_{th} and B_{VT} used in Takeuchi Plot.
(2) Percentage changes of B_{VT} with temperature.

MODE \ PAD	Body	Substrate
A	Floating	Floating
B	Ground	Floating
C	Floating	Ground

Table 2 Three operation modes for V_{th} variation measurement of SOI and SSOI devices.

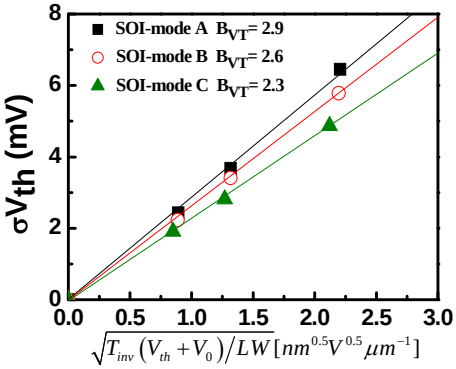


Fig. 5 Comparison of σVth values for three different operation modes of SOI nMOSFETs.

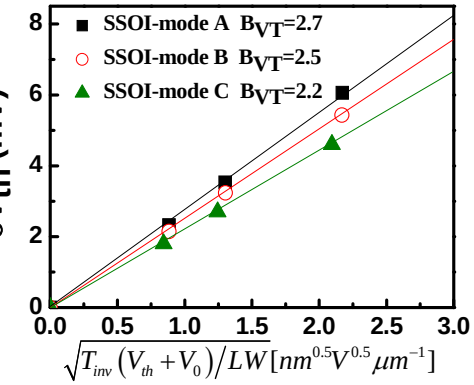


Fig. 6 Comparison of σVth values for three different operation modes of SSOI nMOSFETs.

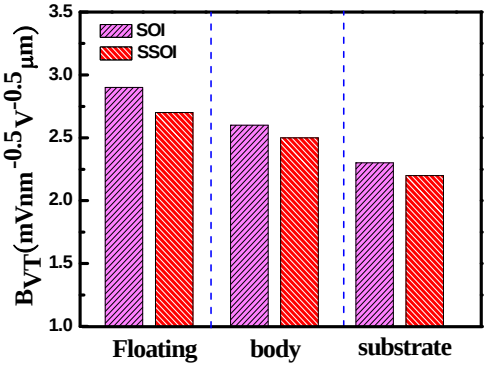
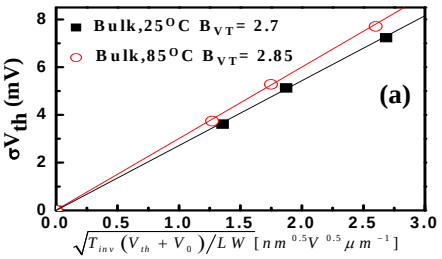
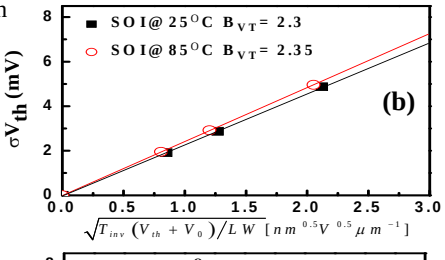
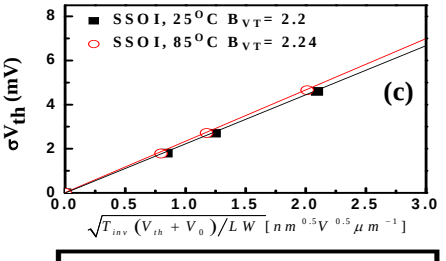


Fig. 7 Comparison of B_{VT} values for three different operation modes of SOI and SSOI nMOSFETs.







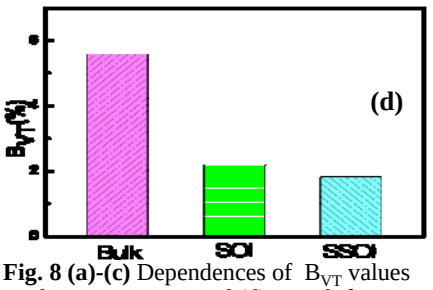


Fig. 8 (a)-(c) Dependences of B_{VT} values on the temperature, and (d) B_{VT} shift at 25°C and 85°C for Bulk, SOI and SSOI nMOSFETs.

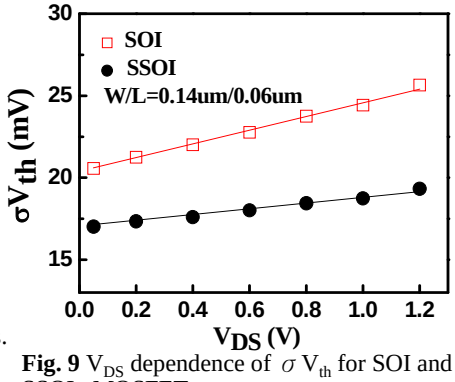


Fig. 9 V_{DS} dependence of σ V_{th} for SOI and SSOI nMOSFETs

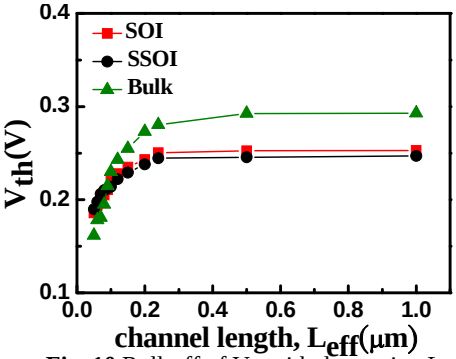


Fig. 10 Roll-off of V_{th} with decreasing L_{eff} for Bulk, SOI, and SSOI nMOSFETs.