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InGaAs and InGaAs-On-Insulator *n*-Channel MOSFETs Fabricated by Self-Align Gate First Process with Ni/Al_2O_3 Gate Stacks

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1. Introduction

III-V semiconductors have attracted attention because of their high electron mobility and low effective mass to overcome physical limits of Si CMOS device scaling. In order to introduce III-V MOS technologies into the Si CMOS platform, it is necessary to integrate III-V channels with Si substrates and to employ the Si standard processes with a minimal addition of new processes. From this viewpoint, the application of a metal-gate/high-k (MG/HK) gate stack technology under the self-align gate first process is mandatory. There have been several reports on MG/HK InGaAs MOSFETs fabricated by the self-align gate first process [1-3]. Here, the compatibility of the thermal stability of MG/HK InGaAs MOS interfaces and the source/drain (S/D) activation annealing is still a strong concern. As for the III-V MOSFET formation on Si substrates, we have already proposed and demonstrated the high performance of III-V-on-insulator (III-V-OI) MOSFETs on Si substrates fabricated by the direct wafer bonding technology under back gate configuration [4,5]. However, III-V-OI MOSFETs under the self-align gate first MG/HK gate stack process have not been reported yet. In this work, for the first time, we report on the performance of the InGaAs-OI nMOSFETs on Si substrates fabricated by self-align gate first process.

2. Experiments

The fabrication process is shown in Fig. 1. The fabrication flow for bulk InGaAs MOSFETs is the following. A 300-nm-thick $In_{0.53}Ga_{0.47}As$ layer which was doped with Zn of $N_A = 3\times10^{16}$ cm^{-3} was grown on an InP (001) wafer by MOVPE. After pretreatment with NH_4OH and $(NH_4)_2S$ solutions, 10-nm-thick Al_2O_3 layer was deposited by atomic layer deposition (ALD). Ni gate electrode was deposited by electron-beam evaporation. Si ions were implanted for S/D region with 2×10^{14} cm^{-2} at 15 keV. For S/D region formation, rapid thermal annealing (RTA) for activation was done at 450, 500, 550, 600, and 650 ºC for 10 s. Au-Ge and Au-Zn were used for S/D contact and back contact, respectively.

As for fabrication of InGaAs-OI MOSFETs, on the other hand, an $In_{0.53}Ga_{0.47}As$-on-Si wafer with a 44-nm-thick ALD-Al_2O_3 BOX layer, fabricated by the direct wafer bonding process, was used [5]. Fig. 2 shows a schematic cross section of the fabricated InGaAs-OI MOSFET and a photograph of a 2-inch $In_{0.53}Ga_{0.47}As$-on-Si wafer. The fabrication process and conditions were almost the same process with bulk MOSFETs. Here, RTA for activation was performed at 600 ºC for 10 s, which is the temperature for minimizing the off current (I_{off}), as described later.

3. Device characteristics of bulk InGaAs MOSFET

The *I-V* characteristics of *p-n*$^+$ junctions in S/D regions with different activation temperatures are shown in Fig. 3. It is found that the I_{off} with RTA at 550 and 600 ºC have the lowest value, while the on-currents (I_{on}) are not significantly dependent. The I_{on}/I_{off} ratio amounts to around ~10^4 at 550 and 600 ºC. The I_D-V_D and I_D-V_G curves of the fabricated MOSFETs with the RTA at 600 ºC are shown in Figs. 5 and 6, respectively. We have confirmed the normal MOSFET operation with the I_{on}/I_{off} ratio of 9×10^3. The I_D-V_G curve exhibits the lowest leakage current and the maximum value of I_{on}/I_{off} ratio. Also, subthreshold swing (*S.S.*) and resulting D_{it} values in this device are 140 mV/decade and 4.3×10^{12} eV^{-1}cm^{-2}, respectively, as shown in Fig. 7. Fig. 8 shows the μ_{eff}-E_{eff} curves as a parameter of the RTA temperature. It is found that the peak mobility is 935 cm^2/Vs with RTA at 500 ºC.

4. Device characteristics of InGaAs-OI MOSFET

Figure 9 shows I_D-V_G curves with V_{sub} of -2 V. The normal MOSFET operation and a large I_{on}/I_{off} ratio of around 5×10^4 are observed. Here, the back interface between InGaAs and BOX is weakly inverted because of the heavily *n*-type doped Si substrate. Thus, application of negative V_{sub} effectively can cut off the leakage current through the back channel, as clearly seen in the V_{sub} dependence of I_D-V_G curves in Fig. 10. It is found that I_{off} has a minimum value at V_{sub} value of -2 V. Also, the V_{TH} shift and *S.S.* the saturate for V_{sub} lower than -2 V, which is attributable to the formation of the hole inversion layer at the back interface. This fact allows us to accurately determine the electric field across the thin body InGaAs channel and resulting E_{eff}. It is found from the μ_{eff}-E_{eff} curve of Fig. 11 that InGaAs-OI MOSFET exhibits the peak mobility of 934 cm^2/Vs and the enhancement factor of 1.5 against the Si universal mobility at E_{eff} of 0.16 MV/cm.

5. Conclusions

We have demonstrated the operation of bulk InGaAs *n*MOSFETs fabricated by self-align gate first process, where the I_{on}/I_{off} ratio and the peak mobility are 9×10^3 and 935 cm^2/Vs, respectively. Also, the high performance of InGaAs-OI *n*MOSFETs with the high electron mobility of 934 cm^2/Vs and with the I_{on}/I_{off} ratio of 5×10^4, which were also fabricated by the self-align gate first process, have been successfully demonstrated for the first time. This indicates that III-V-OI MOSFETs on Si, fabricated by direct wafer bonding, is a quite promising MOSFET structure for future technology nodes.

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References [1] T. D. Lin *et al.*, APL 93, 033516, 2008. [2] J. Q. Lin *et al.*, IEEE IEDM, Tech. Dig., 401, 2008. [3] H-C. Lin *et al.*, Microelectronic Engineering, 86, 1554, 2009. [4] M. Yokoyama *et al.*, APEX, 2, 124501, 2009. [5] M. Yokoyama *et al.*, APL, 96, 142106, 2010.

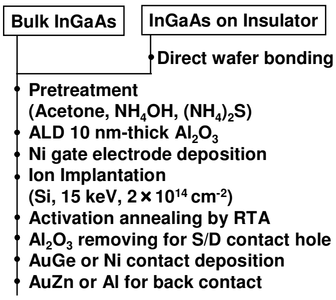

Fig. 1 Fabrication process flow of self-align gate first bulk III-V *n*MOSFETs and III-V-OI *n*MOSFETs.

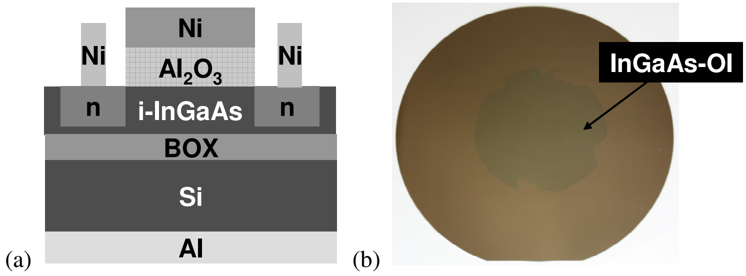

Fig. 2 (a) Schematic cross section of InGaAs-OI MOSFET. (b) A photograph of an $In_{0.53}Ga_{0.47}As$-on-Si wafer. A 2-inch InGaAs layer with an ALD-Al_2O_3 BOX layers is bonded on a 4-inch Si wafer.

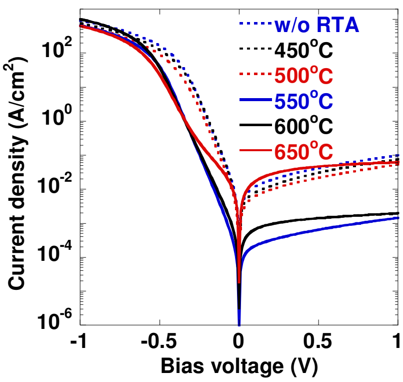

Fig. 3 RTA temperature dependence of *I*-*V* curves of *p*-n^+ junctions.

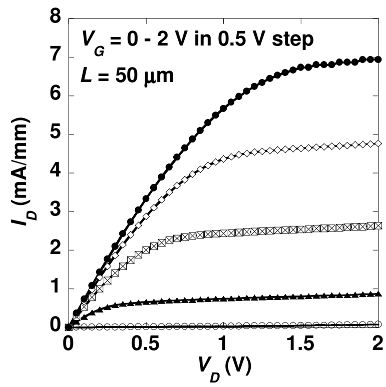

Fig. 4 I_D-V_D curves of bulk InGaAs MOSFET with RTA at 600 ºC.

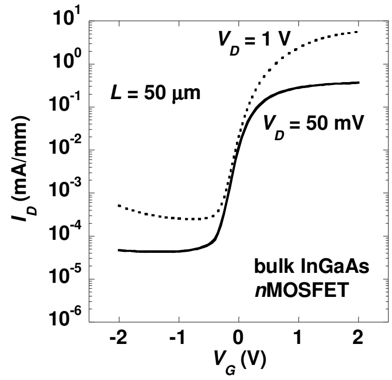

Fig. 5 I_D-V_G curves of bulk InGaAs MOS-FET with RTA at 600 ºC.

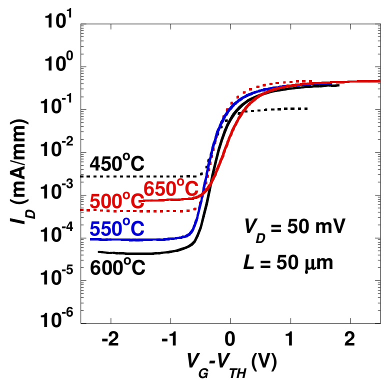

Fig. 6 RTA temperature dependence of I_D-(V_G-V_{TH}) curves of bulk InGaAs MOS-FETs.

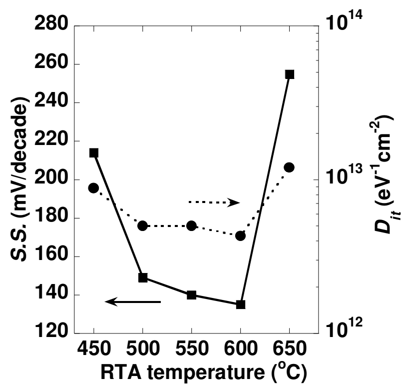

Fig. 7 RTA temperature dependence of the *S.S.* and D_{it} values. The D_{it} values were es-timated from the *S.S.* values.

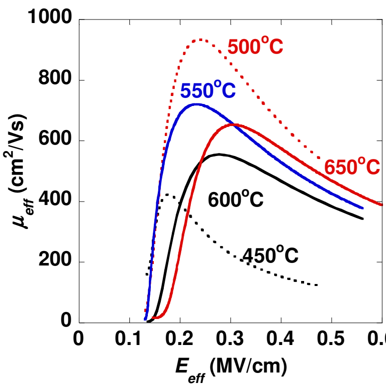

Fig. 8 RTA temperature dependence of μ_{eff}-E_{eff} curves of bulk InGaAs MOSFETs.

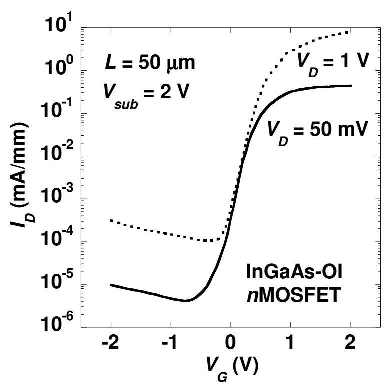

Fig. 9 I_D-V_G curves of the InGaAs-OI MOS-FET with V_{sub} of -2 V applied.

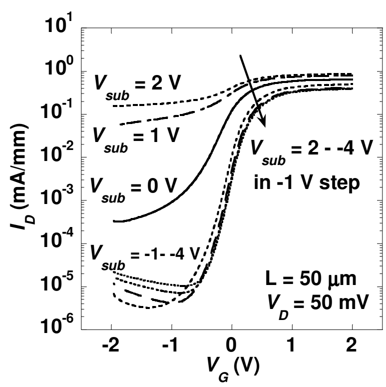

Fig. 10 V_{sub} dependence of I_D-V_G curves of the InGaAs-OI MOSFET.

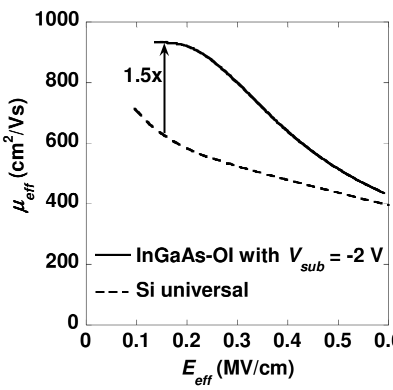

Fig 11. μ_{eff}-E_{eff} curves of InGaAs-OI MOS-FET and Si universal. The peak mobility is 934 cm^2/V at E_{eff} of 0.16 MV/cm.