

# Impedance analysis of controlled-polarization-type ferroelectric-gate TFT using RC distributed constant circuit

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## 1. Introduction

Recently, ferroelectric-gate field-effect transistors (FETs) have attracted much attention because they have several advantages such as nonvolatility, fast and nondestructive readable operation, capability of high-density integration and low power consumption. The ferroelectric-gate FETs with a metal-ferroelectric-insulator-silicon structure have been developed and nonvolatile memory operation and long memory retention time have been reported. However, metal-ferroelectric-insulator-silicon structure have disadvantage on lowering the operation voltage due to the existence of the insulator layer. Hence, the use of an oxide semiconductor was proposed as another way to obtain a good interface between ferroelectric and semiconductor. However, ferroelectric-gate TFT using oxide semiconductor channel usually operates at accumulation-depletion mode, because most of oxide semiconductor dose not form inversion layer. This indicates that the charge density of the oxide semiconductor in depletion condition is much lower than the spontaneous polarization of typical

ferroelectric material. It can be expected that this charge mismatch causes difficulty of polarization switching of the ferroelectric layer and so on.

To solve the issue of charge mismatch, we propose novel ferroelectric-gate thin films transistors (TFTs) using an interaction between the spontaneous polarization of a polar semiconductor ( $P_{SPS}$ ) and a ferroelectric layer ( $P_{SFE}$ ), which is named a controlled-polarization-type ferroelectric-gate TFTs [1,2]. The controlled-polarization-type ferroelectric-gate TFTs which have metal-ferroelectric-semiconductor (MFS) structure were fabricated using ZnO channel as the polar semiconductor and an YMnO<sub>3</sub> film as the ferroelectric gate. Although nonvolatile memory operation is observed on the ferroelectric-gate TFT with ZnO/YMnO<sub>3</sub> structure [1,2], the state of the channel and distribution of the carrier concentration was not revealed.

In case of TFTs with a paraelectric gate insulator, the carrier concentration in the channel changes gradually from source to drain. On the other hand, in case of TFTs with a ferroelectric gate insulator, the carrier concentration is controlled by  $P_{SFE}$ , which indicates the carrier concentration depends on the domain structure of the ferroelectric layer. Therefore, it can be expected that the carrier concentration and transistor operation of TFTs with a ferroelectric gate insulator is more complicated than that with a paraelectric gate insulator. To investigate the distribution of the carrier concentration in the channel of the ferroelectric-gate TFT with ZnO/YMnO<sub>3</sub> structure with a ferroelectric gate insulator, impedance spectra of was measured and analyzed using TFT model shown in Fig. 1(a), because TFT express by RC distributed constant circuit at high frequency region.

## 2. Results and Discussion

The impedance spectra for the TFT model with the RC distributed constant circuit shown in Fig. 1(a) was calculated by SPICE. The obtained impedance spectrum is analyzed by the equivalent circuit of the TFT model shown in Fig. 1(b) [3].  $C_S$  and  $C_D$  in the equivalent circuit correspond with the capacitances of the channel region near source and drain electrodes. Since the capacitance of the channel in Fig. 1(a) is a total of  $C_S$  and  $C_D$ , the change of the distribution of the carrier concentration can be evaluated by the ratio of  $C_S$  and  $C_D$ . Figure 2 shows the calculated results of  $C_S$ ,  $C_D$  and the channel resistance at various channel condition. When the channel resistance is

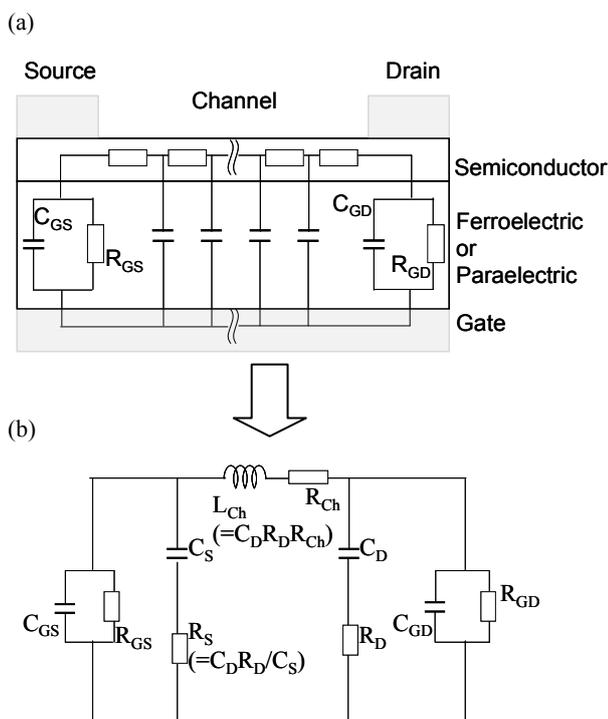


Fig.1 RC distributed constant circuit and equivalent circuit

low (Fig.2(a)), the ratio of  $C_S$  and  $C_D$  are 82 % and 18 %, respectively. This result indicates that the region corresponding to  $C_S$  expands when the channel resistance is low. Moreover, the ratio of  $C_S$  and  $C_D$  were calculated in the cases of high channel resistance (Fig.2(b)), gradual change of resistivity, which corresponds the channel of the paraelectric-gate TFT (Fig.2(c)), and steep change of resistivity, which corresponds the channel of the ferroelectric-gate TFT (Fig.2(d)). The results indicate that the  $C_S$  region expands when the channel resistance is low, and the  $C_S$  region shrinks when the channel has high resistance or gradual change of resistivity. When the channel has steep change of resistivity, the  $C_S$  region of element shrinks greatly than the other channel conditions. Therefore it was found that this change of  $C_S$  is peculiar phenomenon in ferroelectric-gate TFT.

Then, impedance spectra of the ferroelectric-gate TFT with ZnO/YMnO<sub>3</sub>/Pt/YSZ structure were measured in Fig. 3(a). The carrier concentration of ZnO was  $1.5 \times 10^{16} \text{ cm}^{-3}$ . The gate voltage was changed from -4 V to 4 V, and the impedance spectra were measured between the source and gate electrodes. The fitting was carried out using the equivalent circuit shown in Fig. 1(b). The result is shown in Fig. 3. The sum of  $C_S$  and  $C_D$  is not constant because relative permittivity of ferroelectric is depends on applied

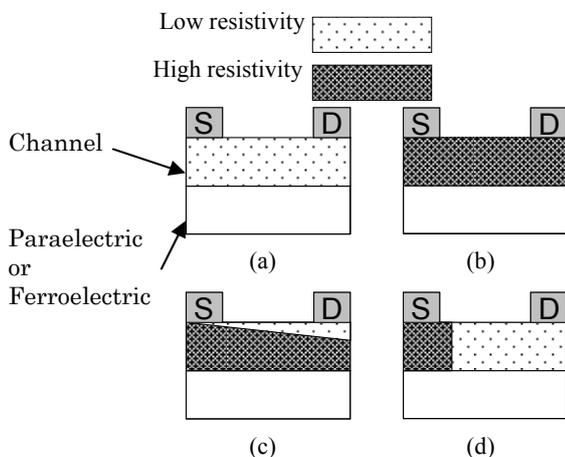
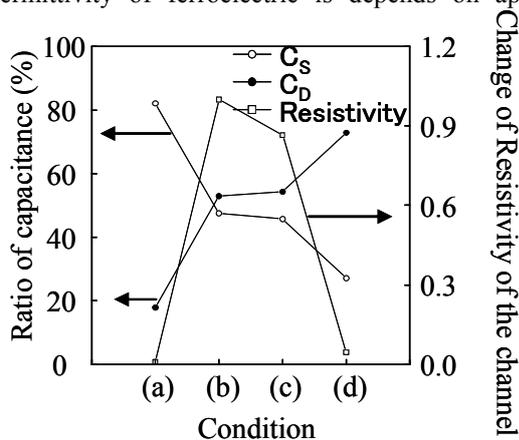


Fig.2 change of  $C_S$  and  $C_D$  when resistance elements in channel are (a) low, (b) high, (c) gradually and (d) steep resistivity

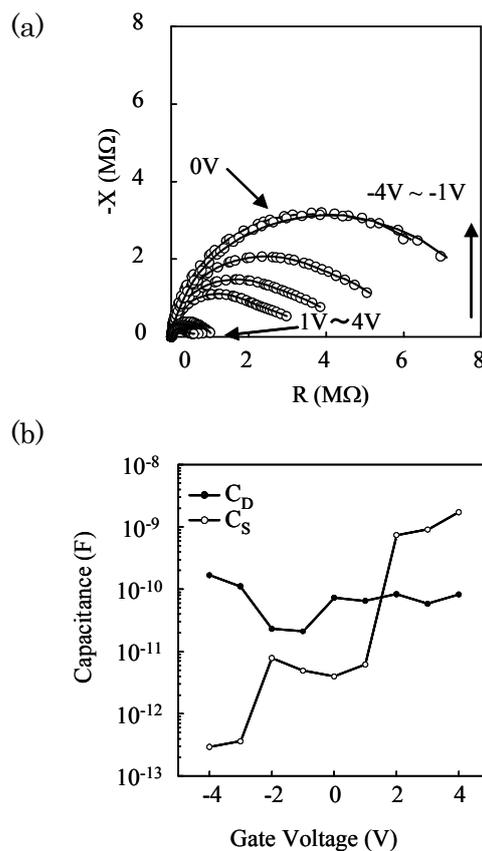


Fig.3 (a) Impedance spectra and fitting results (b) fitting results of  $C_S$  and  $C_D$  in the channel on the gate voltage

voltage and the electrode area expands when channel is accumulated. While  $C_D$  is almost independent on the gate voltage,  $C_S$  decreases with decreasing the gate voltage. The decrease of  $C_S$  at negative gate voltage region indicates that the increase of resistivity in the channel is occurred only at the region near the source electrode, which suggests that  $P_{SFe}$  of YMnO<sub>3</sub> is switched only at the region. On the other hand, the increase of  $C_S$  at positive gate voltage region indicates that the decrease of resistivity in the channel is occurred at entire channel region.

### 3. Conclusions

The impedance analysis using RC distributed constant circuit is applicable to analysis of the channel condition of ferroelectric-gate TFT. The results suggests that the reversal of  $P_{SFe}$  for YMnO<sub>3</sub> was occurred only at the region near the source electrode by negative gate voltage, and entire channel region becomes low resistivity state by positive gate voltage.

### References

- [1] T. Fukushima, T. Yoshimura, K. Masuko, K. Maeda, A. Ashida, and N. Fujimura, Jpn. J. Appl. Phys. 47, 8874 (2008)
- [2] T. Fukushima, T. Yoshimura, K. Masuko, K. Maeda, A. Ashida, and N. Fujimura, Thin Solid Films 518, 3026 (2009)
- [3] J. R. Hauser, IEEE Trans. Electron Device, ED-12, 605 (1965)