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High Efficiency Charge Storage Layer for MLC NAND Non-Volatile Memory

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1. Introduction

Recently, multi-level cell (MLC) as a promising technique has been researching to increase the storage density of SONOS-type NAND non-volatile memory [1]. However, the main challenge of MLC operation is an electrical reliability problem because charge data retention and device endurance influence discrimination of multi bit. Therefore, the level of voltage offset between state and state (11, 10, 01, and 00) plays one of the key factors for MLC [2]. To significantly differentiate between the voltage offset levels, increase of charge storage is an efficiency solution to provide more conspicuous offset voltage among states.

This paper presents a novel ion bombardment method to enhance the efficiency of charge storage layer. In addition, a sol-gel derived high-*k* material was used as the charge storage layer because a relative larger trapping density of the sol-gel derived high-*k* storage layer has been widely investigated than those of the other deposition methods [3-5]. Compare to other deposition methods, the benefits of sol–gel method are relatively cheap, simplicity, good uniformity, and mixing a variety of materials without restriction. The electrical properties of the ion bombardment treated and sol-gel derived charge storage layer are demonstrated in terms of memory window, program speed, charge retention, and sensing window. The good electrical performance is attributed to the effects of high efficiency charge storage (150% increase of trapping density) by ion bombardment treatment.

2. Experiment

This study adopted a Si_3N_4/SiO_2 stacked layer as the equivalent tunneling layer. Firstly, a 2nm thick silicon oxide was thermal grown followed by a 2nm thick silicon nitride deposited by LPCVD. Subsequently, argon ions bombardment was carried out onto silicon nitride surface by HDPCVD (RF power: 200W, DC power: 20W, Temperature: 375℃). Afterward, a 15 nm HfO_2 was deposited by sol-gel spin-coating method as a charge storage layer. The Hf: IPA solution (molar ratio: 1:1000) was coated by using a spin-coater at 3000 rpm for 60 sec at 25℃. The as-deposited thin film was initially backed at 200℃ for 10 min to perform densification, followed by high-*k* RTA for 1 min in an O_2 atmosphere to form the HfO_2 charge trapping layer. A 30nm thick blocking oxide was deposited at 250℃ by PECVD. Aluminum electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/HfO_2/nitride/oxide/silicon (MOHNOS) capacitor structure NAND-type non-volatile memory.

3. Results and Discussion

Fig.1 depicts the program/erase characteristics of the MOHNOS memory with and without ion bombardment treatment. It is seen in the figure, the sol-gel derived high-*k* charge storage layer exhibits a highly trapping efficiency which in terms of fast program speed (V_{FB} shift of 2.75 V at 10^{-5} s) and a wide memory window of 4.25 V. Furthermore, a drastic improvement of program speed (V_T shift of 5.25 V at 10^{-5} s) and a relative wide memory window of 7.5 V were achieved by using the ion bombardment treatment onto the Si_3N_4/SiO_2 stacked tunneling layer. In additions, the charge detrapping efficiency was improved nearly 100 times by using the ion bombardment treatment as shown in the inset of Fig. 1. It can be seen that the sol-gel derived sample with ion bombardment treatment only needed an erase time of 10^{-3} sec to completely remove the total charge storage. On the contrary, the sample without ion bombardment had to need 10^{-1}sec. Atomic force microscope (AFM) and discharge-based multi-pulse (DMP) technique [6] were used to analysis the effect of the ion bombardment. Fig. 2 shows the difference in nitride surface roughness between samples with and without ion bombardment. In contrast to the control sample (rms of 0.241 nm), a relative rough surface with rms of 0.398 nm was observed for the sample under ion bombardment. It implies that the ion bombardment process damaged the nitride surface and increased the

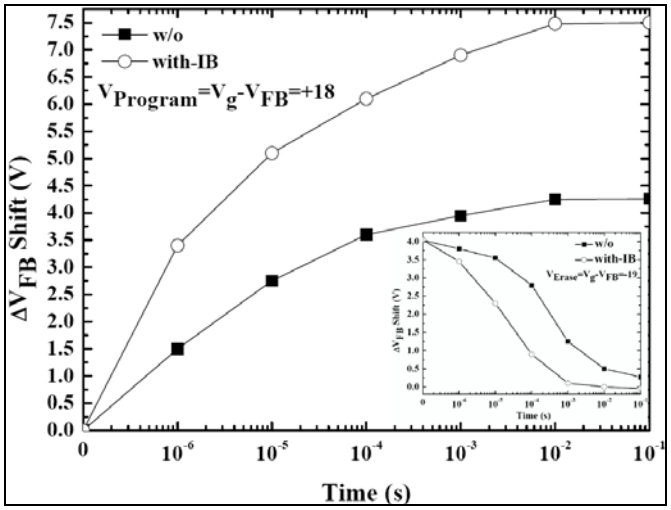
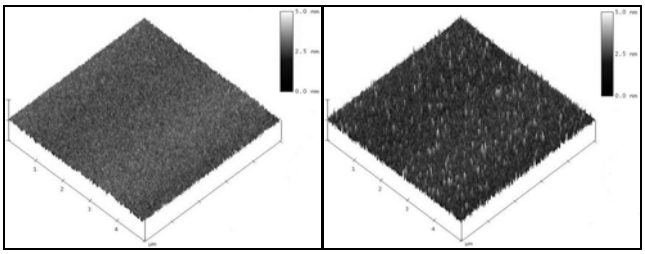
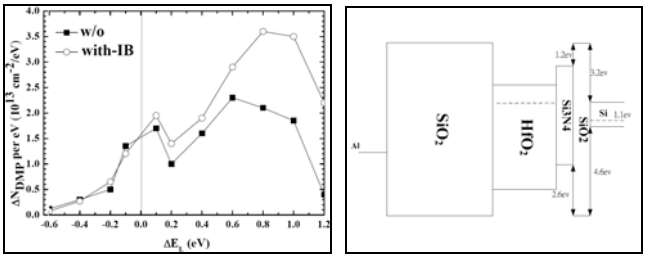


Fig. 1 Program and erase characteristics under conditions of $V_{Program}=V_g-V_{FB}$= +18V and $V_{Erase}=V_g-V_{FB}$= -19V.



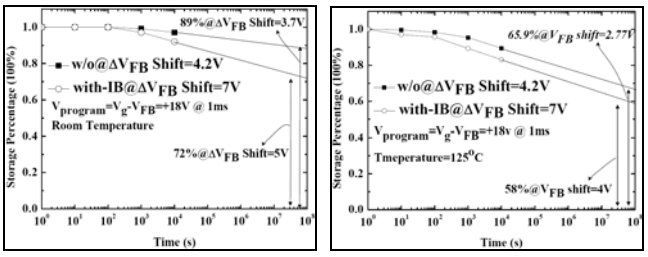
(a) (b)

Fig. 2 AFM images of surface roughness of Si_3N_4 (a) without and (b) with ion bombardment.



(a) (b)

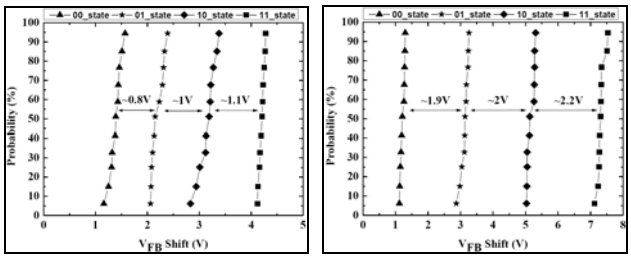
Fig. 3 (a) Trap density per eV vs. energy level for the MOHNOS memories measured by the DMP method. (b) Energy band diagram of the MOHNOS structure.



(a) (b)

Fig. 4 Retention characteristics of the MOHNOS memories at measurement temperatures of (a) room temperature and (b) 125℃.

surface roughness. Furthermore, DMP analyses illustrate the evidence of additional trapping sites created by the ion bombardment as shown in Fig. 3. The vertical dot line shown in Fig. 3(a) and the horizontal dot line shown in Fig. 3(b) represent the relative energy level corresponds to the conduction band of Si substrate. Fig. 3(a) depicts that ion bombardment increased trapping sites (ca. 150 %) within the charge storage layer and the distribution of the additional trap sites almost located at the shallow energy level (between $\triangle E_L$= 0.1eV and 1.2eV). The additional shallow trapping sites widen the memory window and yielded a high P/E speed as shown in Fig.1. Fig. 4 shows the data retention of MOHNOS memories. The normalized V_{FB} shift is defined as the ratio of the V_{FB} shift at the time of interest and at the beginning. It is seen that a robust data retention characteristic has been achieved by the sol-gel derived charge storage layer. Extrapolating to 10 years, a highly reliable retention properties with only 11% and 28% charge lose will be performed at room temperature and 125℃ respectively. Although the ion bombardment damaged the nitride surface and resulted in a relative large charge lose as compared to that of without ion bombardment. The device still yielded a reasonable 10-year data retention characteristic (34.1% and 42% charge lose at room temperature and 125℃ respectively) due to the robust sol-gel derived charge storage layer. Fig. 5 shows cumulative distributions of sol-gel derived NAND-type memories with/without ion bombardment for MLC operation. The sensing windows of the sol-gel derived sample between levels of 11/10/01/00 are 1.1V, 1V, and 0.9V, respectively. As discussed in Fig.1, the ion bombardment treatment improved the trapping efficiency. Therefore, relative wide sensing windows of 2.2V, 2V, and 1.9V between levels of 11/10/01/00 can be achieved by using the ion bombardment treatment as shown in Fig. 5(b).



(a) (b)

Fig. 5 Cumulative distribution of sensing window for MLC operation. (a) sol-gel derived NAND-type memories and (b) sol-gel derived storage layer and ion bombarded NAND-type memories.

4. Conclusion

In this work, we succeeded in combining a sol-gel derived high-*k* material with ion bombardment method to fabricate the high efficiency charge storage. This high efficiency charge storage significantly increased sensing window between state and state (11, 10, 01, and 00) to improve reliability for NAND-type MLC operation. We also verified that the ion bombardment improved electrical properties in terms of memory window (~74%), program speed (~90%), and erase speed (~100 times). DMP analysis confirmed that the good electrical performance was attributed to the effects of high efficiency for charge storage (150% increase of trapping density). Therefore, the sol-gel derived storage layer with ion bombardment seems to be a promising candidate for MLC non-volatile memory in the future.

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