Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp327-328

A Low Loss High Selectivity Compact On-Chip Bandpass Filter for 60 GHz Millimeter Wave CMOS SoC Solution Using Patterned Ground Shields

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1. Introduction

In recent years, on-chip millimeter wave devices have attracted attention of many researchers and engineers due to the availability of the frequency bands at 60 GHz without license. CMOS is particularly attractive for 60 GHz band applications because of the low cost and its potential of integration with back-end circuits, enabling easy systems-on-chip (SoC) solution. The half-wavelength of a 60 GHz electromagnetic wave in vacuum is 2.5 mm, and this will further be reduced in dielectric medium by the square root of its relative permittivity. Therefore, system-on-chip solution including on-chip passive devices like filter and antenna is possible at 60 GHz. Unfortunately, the conductor and dielectric losses downplay the performance of the on-chip passive devices significantly at 60 GHz-band.

In this paper, a low loss and small size on-chip bandpass filter (BPF) is proposed and implemented in 0.18 μm CMOS technology. The proposed BPF employs two-stage coupled ring resonators and patterned shield ground to reduce the insertion loss and chip size significantly.

2. Design of On-chip Bandpass Filter in CMOS

A conventional on-chip BPF has large on-chip area (more than 1 mm^2) and insertion loss is higher than 5 dB [1] [2]. To overcome these problems, we proposed two-stage coupled ring resonators BPF. One of the difficulties in realizing the coupled ring resonators filter is to identify and control the required electric and magnetic couplings between the resonators [3].

Fig. 1 shows the proposed square open-loop resonator BPF where total length (l_1+l_2) is half-wavelength of the guided waves at the center frequency (60 GHz). In Fig. 1(b), its equivalent circuit is shown from where the Admittance (**Y**) matrix is derived as

$$|\mathbf{Y}| = \begin{vmatrix} j\omega C & -j\omega C_m \\ -j\omega C_m & j\omega C \end{vmatrix} \qquad (1)$$

In figure, the electric coupling between the two resonant loops is represented by an admittance inverter $\boldsymbol{J}$ =ωC$_m$. The electric coupling K$_E$ is determined by

$$K_E = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2} = \frac{C_m}{C} \qquad (2)$$

Where f_m and f_e are high an low resonant frequencies. The tapping positions also affect the couplings between two resonators. The over-coupled condition is given by

$$K > \frac{1}{Q_0} + \frac{1}{Q_e} \qquad (3)$$

where K is the coupling coefficient, Q_0 is the unloaded Q of either of the two resonators, and Q_e is the external Q. The measured external Q is given by

$$Q_e = \frac{f_0}{\Delta f_{\pm 90^\circ}} \qquad (4)$$

where $\Delta f_{\pm 90^\circ}$is the bandwidth about the resonant frequency, over which the phase varies from -90° to +90°.

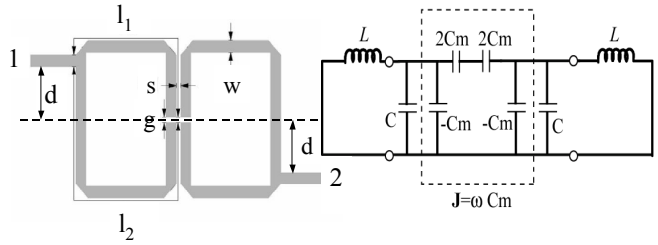

Fig. 1. Proposed BPF employing two-stage coupled ring resonators (a) and its equivalent circuit exhibiting electric coupling (b).

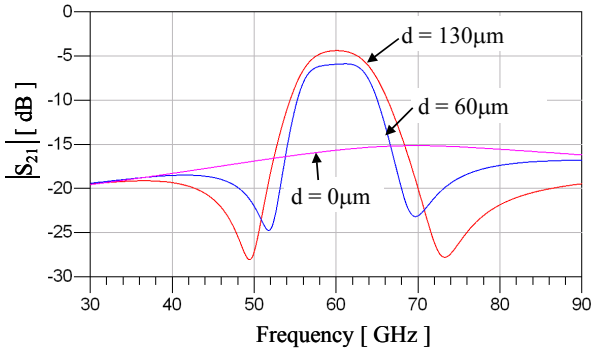

Fig. 2. Comparison of insertion losses simulated by EM simulator for different tapping positions with coupling gap s = 5 μm.

Fig. 2 shows the comparison of simulated S21 based on the tapping positions at a distance d from the center of the resonators to the input and output ports. When d becomes large, the external Q becomes larger. The larger external Q allows the filter to approach the overcoupled condition in Equation (4). In addition, for a shorter d, the two transmission zeros appear close to the passband, providing a high selectivity nearby the passband. But this may easily induce

an overcoupled condition. When d becomes zero (i. e. center position), only anti-resonance will appear causing disappearance of the resonance as shown in Fig. 2. Beyond the coupling effects caused by the tapping positions, the coupling gap *g* also influences the coupling between two resonators. Therefore, to avoid over-coupling, the proper tapping positions and gap size should be carefully chosen. In this design, d = 130μm, s = 5μm was the designed values to allow the low insertion loss and two transmission zeros near the pass band to improve the frequency selectivity.

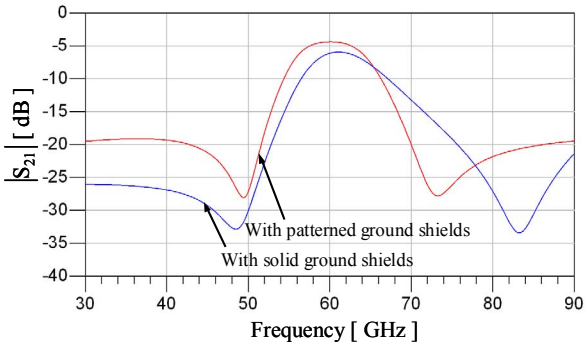

Fig. 3. Comparison of insertion losses (simulated by EM simulator) with and without patterned shield ground.

A patterned ground shields improves the Q and isolation of an on-chip inductor [4]. Furthermore, with the addition of the patterned ground shield, slow wave effect can be reproduced which results in the BPF size to be more compact. Therefore, the patterned ground shield is used to improve the insertion loss of the BPF. Fig. 3 shows the simulated results of $|S_{21}|$ of the BPF with patterned ground shield and with solid ground shield which illustrates that the insertion loss of the BPF with patterned ground shield is improved by 1.8 dB at 60 GHz.

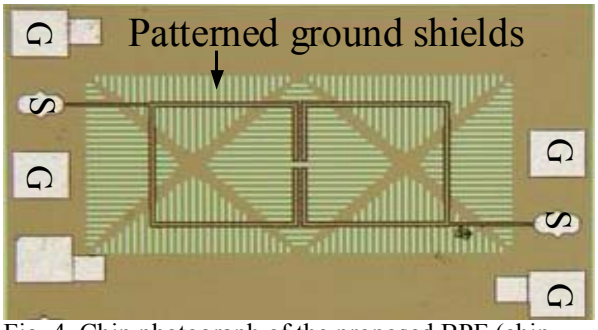

Fig. 4. Chip photograph of the proposed BPF (chip size=1000 μm x 450 μm without pads).

3. Measurement and Discussion

The designed BPF is implemented in 0.18 μm CMOS technology. Fig. 4 shows the chip photo of the proposed BPF with patterned ground shields. On-wafer measurement was carried out by Agilent VNA (E8361C PNA series), which offers the measurement up to 70 GHz only. Therefore, in the measurement shown in Fig. 5, the measured results could not provided beyond 70 GHz though the designed results were well reproduced by the measurement up to 70 GHz giving the solid evidence of the proposed technique. In this paper, 1.8 dB improvement of insertion loss was achieved by the pattern ground shields, and 40% reduction in chip size due to the slow wave effect of the patterned ground shields.

The measured insertion loss and return loss of the proposed BPF are 3.1 dB and greater than 25 dB at 60 GHz, respectively which are the significant improvement over those reported in CMOS BPF [1] [2] and MEMS BPF [5] at millimeter wave band. The core size of the BPF is only 0.45 mm^2 which is almost 50% smaller than the recent CMOS BPF [1] [2] and 98% smaller than MEMS BPF [5].

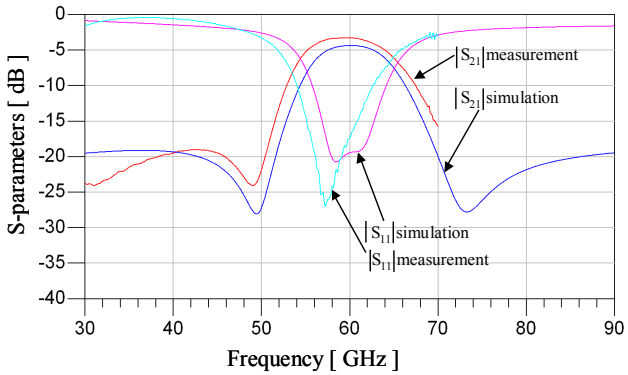

Fig. 5. Comparison of S-parameters of the proposed BPF.

4. Conclusion

We proposed on-chip BPF for 60 GHz band applications based on two-stage coupled ring resonators and patterned ground shield in 0.18 μm CMOS technology. First, low insertion loss was realized by the trade-off between coupling and frequency selectivity by creating two transmission zeros near the passband realized by tapping position and further improved by using the patterned ground shields. The proposed BPF outperforms the previous millimeter-wave BPFs [1] [2] [5] significantly in performance and size.

Acknowledgements

We would like to express sincere thanks to Prof. A. Sanada of Yamaguchi University and Prof. K. Okada of Tokyo Institute of Technology for their help during the measurement. This work was partially supported by VDEC in collaboration with Cadence Design Systems, Inc and Agilent Tech.

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