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A Multiple Time Programmable On-chip Trimming Technique for CMOS Bandgap Reference Circuits

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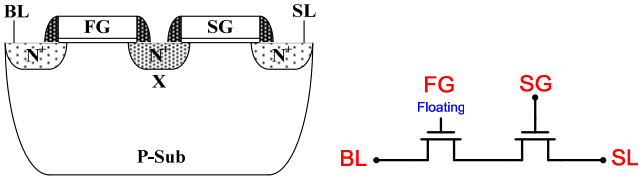
1. Introduction

The bandbap reference (BGR) circuits generating a constant voltage independent of temperatures and supply voltages are widely used in many integrated circuits (IC), such as non-volatile memories, analog to digital converters, power supplies, liquid crystal display (LCD) drivers, and so forth. However, process variation and mismatch induce some variations of the reference voltages. They could reach ±100mV if the BGR voltage is set at 1.2V.

Trimming after chip fabrication is the practical method to narrow down the variations. Laser trimming is the most popular approach in industries, but it is occupied large chip area and the special laser machine is required [1][2]. An alternative technique uses poly fuses [3][4] to trim the reference voltage. They can be electrically programmed once, and thus termed as one time programmable (OTP) memory devices, but the area per fuse could be several hundred μm^2. This paper proposes a new trimming technique employs multiple time programmable (MTP) memory devices [5] in the standard 0.35μm CMOS technology to reduce reference voltage variations. The area per device is only tens μm^2 and could be reprogrammed and erased many times for more flexibility

2. Operation of Trimming Switches

Fig. 1(a) shows the cross section of MTP device [5] to be used as the trimming switch. Fig. 1(b) is the schematic symbol of the device. It consists of two NMOS transistors with grounded P-substrate using 0.35μm CMOS technology. The three electrodes BL, SG and SL are applied to some bias conditions for program, erase and read operations as illustrated in Table I. The floating gate (FG) node and Node X between the two transistors are floated.



(a) Cross sectional view (b) Schematic symbol

Fig. 1 The MTP device used as a programmable trimming switch

Table I The bias conditions of the MTP device

	BL		SG		SL
	Select	Unselect	Select	Unselect	
Program	7V	0V	4V	0V	0V
Erase	7V	0V	1V	0V	0V
Read	0V	0V	2V	0V	1V

Before program, the current from SL to the grounded BL is very small with the read condition. By applying the program condition on the MTP device for 10ms, the read current could reach more than 80μA due to channel hot holes injecting into the floating gate (FG). On the other hand, the channel hot electrons can be injected into the FG node to recombine with the holes using the erase condition for 5ms, and the read current become negligible. The similar procedures can be repeated. That is why it named MTP and can be applied to trim circuits with more flexibility.

3. Bandgap Circuit with Trimming Switches

Four MTP devices were designed to trim the conventional BGR circuit [6] as illustrated in Fig. 2. V_{BGR} is the bandgap reference voltage which has more variations between different chips. V_{REF} is the reference voltage with much less variations after trimming.

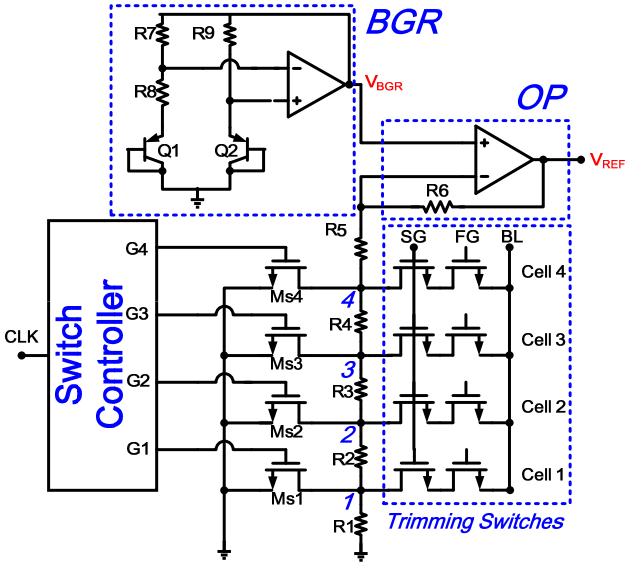


Fig. 2 The complete voltage reference circuit with four trimming switches to fine tune V_{REF}.

In Fig. 2, one of the four trimming switches may be programmed like anti-fuse to set one of the four nodes (Node 1 to Node 4) to be grounded. For example, if cell 2 needs to be programmed, BL and SG are set to 7V and 4V, respectively, and Ms2 is on with G2=3.3V to make Node 2 grounded. Since the resistor string R_1 to R_5 were selected to be 200kΩ, if some current, such as 5μA, goes through them, the voltage drop could reach 1V! In fact, the program current is higher than 5μA, so the other cells will not be disturbed. After cell 2 is programmed, if Ms1 to Ms4 keep off, and BL and SG are set to 0V and more than 1V, respectively, Node 2 will be very close to 0V due to good conductivity of cell2. Thus, effective resistance of the

resistor string can be adjusted.

Another feature of the proposed trimming technique is the programmed cell can be erased using the bias condition given in Table I in case the user likes to change V_{REF}.

The relation between V_{REF} and V_{BGR} is

$$V_{REF} = V_{BGR} + \frac{R_6}{\sum_{i=k}^{5} R_i} V_{BGR} \quad (1)$$

where k can be selected between 1 to 5 depending on the trimming switches. For example, if cell 3 is programmed, k is 4. If no cells are programmed, k should be 1. In our design, R_6 is 20kΩ which is much smaller than R_1 to R_5 to obtain the small tuning range of about 80mV.

4. Measurement Results

The Circuit in Fig. 2 was fabricated using TSMC 0.35μm CMOS process. Fig. 3 demonstrates the chip photograph with the trimming switches occupied in very small area.

Figs. 4 and 5 are the measured V_{REF} for different V_{DD} at room temperature and different temperatures at V_{DD}=3.3V. Figs. 4(a) and 5(a) show the maximum V_{REF} variation between 6 samples are close to 120mV before trimming. The variation is reduced to 20mV after trimming as demonstrated in Figs. 4(b) and 5(b). Due to some mismatch issues in the circuit, the temperature coefficients in Fig. 5 are higher than expected.

5. Conclusions

An alternative trimming technique for voltage reference circuits using MTP devices is proposed in smaller chip area with more flexibility. The measurement results demonstrate the variation of reference voltages could be reduces from 120mV to 20mV after the proposed trimming method was applied.

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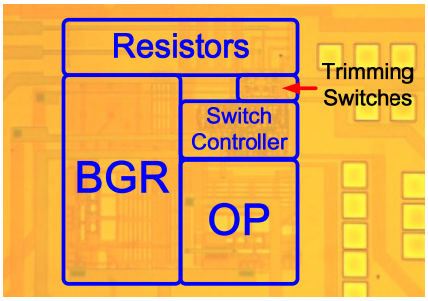

Fig. 3 The chip photograph corresponding to the circuit in Fig. 2 with the trimming switches indicated by the arrow.

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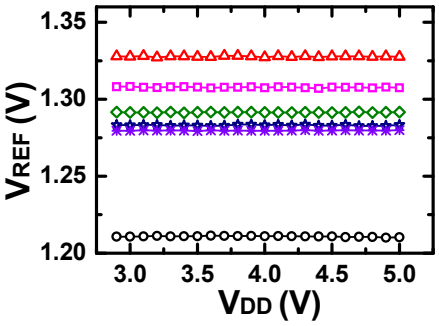

Fig. 4 (a) V_{REF} versus supply voltages before trimming at 25°C

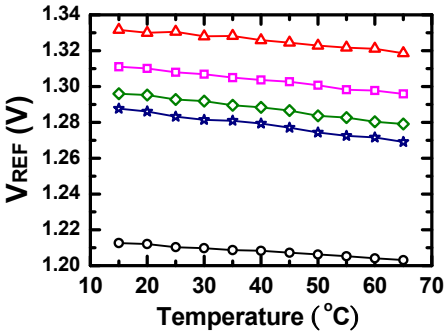

Fig. 5 (a) V_{REF} versus temperatures before trimming for V_{DD}=3.3V

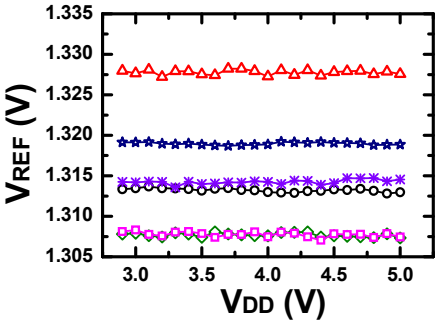

Fig. 4 (b) V_{REF} versus supply voltages after trimming at 25°C

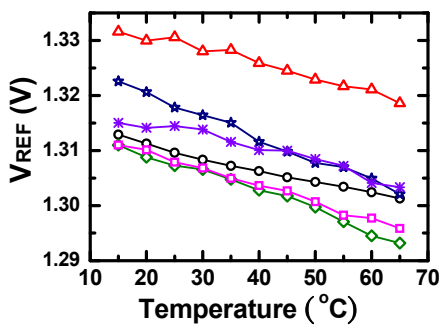

Fig. 5 (b) V_{REF} versus temperatures after trimming for V_{DD}=3.3V