A Sub-nanoampere Two-stage Power Management Circuit in 0.35-μm CMOS for Dust-Size Batteryless Sensor Nodes
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1. Introduction
Wireless sensor nodes with energy harvesting are attracting great interest for “ambient intelligence” [1]. For such networks, one of the most important demands is size reduction of the nodes, and dust-size sensor nodes are expected [2]. Because the size of the energy harvesting block is almost proportional to its power generation ability [3], the dust-size sensor nodes must operate with nano-ampere level energy harvesting [4]. The sensor nodes have to accumulate the energy needed for radio [1] because the generated power is much smaller than the power used for radio. A power management circuit, which monitors the accumulated energy and controls the current flowing into the radio block, is a key circuit determining the minimum current for accumulating because the generated power must be larger than the power consumption of the management circuit. Thus we devised a two-stage power management circuit for sub-nanoampere operation.

2. Architecture
Fig. 1 shows the simulated relation between leakage current and supply voltage for PMOS and NMOS power switches when energy from a generator is accumulated and supplied to radio through the power switches. The leakage current is 0.7 nA for the PMOS switch and 3 nA for the NMOS switch at V_{DD}=2V.

The power switch is usually controlled by a comparator. The transition time of the switch is determined by the comparator current and the parasitic capacitance of the switch. Fig. 2 shows the simulated relation between the transition time and the comparator current for PMOS and NMOS power switches. The operation time of the radio block in the sensor node is expected to be about 100 μs [4]. Thus, if the energy loss with the power switch transition is less than 10% of the energy used for radio, the transition time should be smaller than 20 μs. This means that the comparator current for PMOS and NMOS power switches should be more than 18 and 7 nA, respectively. The summation of the switch leakage and the comparator current is 19 nA for the PMOS switch and 10 nA for the NMOS switch. Thus, a single-stage power management circuit cannot accumulate the energy from a nano-ampere power generator.

We therefore propose the two-stage power management architecture shown in Fig. 3. The first stage accumulates the energy from a nano-ampere power generator and supplies about 100-μA current to the second stage. The second stage accumulates the 100-μA current from the first stage and supplies about 1-mA current to the radio block. The gate width of the first-stage power switch is one order of magnitude smaller than that of the second-stage switch. Thus, the leakage current of the first switch is smaller than 0.1 nA, which is satisfactorily small enough for the sub-nanoampere power management. The transition time of the first switch is estimated to be about 120 μs, but the energy loss with the first-switch transition is about 6% of the energy used for the radio because the supply current is one order of magnitude smaller than that of the second-stage switch.

The voltage-monitoring circuit in the second stage consists of a conventional band-gap reference circuit and consumes several microamperes as shown in Fig. 3. This power dissipation is not important because the second stage operates only when the radio is operating and its power is negligibly smaller than the power consumed by the radio. However, the current consumption of the first stage must be four orders of magnitude smaller than that of the second stage because the first stage must operate all the time.

With a previously proposed technique, the low-power band-gap reference circuit consumes sub-microamperes [6]; that is, the power management block cannot operate with nanowatt-level power. Thus, a novel voltage-monitoring circuit is used for the first stage as shown in Fig. 4. The voltage-monitoring circuit features sub-nanoampere operation, with a series-connection of multiple diode-connected MOSFETs for voltage regulation and a cross-coupled transistor pair for positive-feedback amplification. Initially, the diode-connected MOSFETs are in the “off” state. When VIN applies threshold voltage to each diode, sub-nanoampere current is generated in the voltage-regulating circuit. This current is mirrored to the current source ISNC in the SNC circuit. This causes a current difference in MOSFETs Q1.
and Q2 in the design of the channel width: \( W_{Q2} > W_{Q1} \). This current difference is amplified to voltage signal by the cross-coupled transistor pair and the relationship between voltages Out1 and Out2 is inverted. This differential signal from the voltage-monitoring circuit is converted to a pulse by the hysteresis comparator, which means that the voltage of the accumulated energy reaches the voltage determined by the number of diode-connected MOSFETs. Thus, the proposed circuit can monitor the voltage of the accumulated energy and regulate it with power consumption of sub-nanoampere current.

The input voltage \( V_{IN} \), the first supply voltage \( V_{DD1} \) and the second supply voltage \( V_{DD2} \) were evaluated at the points depicted in Fig. 3. In the simulation, the input current was 1 nA and the first and second off-chip capacitors were 2.2 \( \mu \)F and 0.7 \( \mu \)F, respectively. The interval of the final output (\( V_{DD2} \)) was about 3 hours. Our OOK transmitter [5] can transmit 103-bit data using the \( V_{DD2} \) output.

Fig. 4. Voltage-monitoring circuit in the first stage.

Fig. 5 shows the simulated transition characteristics of the sub-nanoampere two-stage power management circuit. The input voltage \( V_{IN} \), the first supply voltage \( V_{DD1} \) and the second supply voltage \( V_{DD2} \) were evaluated at the points depicted in Fig. 3. In the simulation, the input current was 1 nA and the first and second off-chip capacitors were 2.2 and 0.7 \( \mu \)F, respectively. The interval of the final output (\( V_{DD2} \)) was about 3 hours. Our OOK transmitter [5] can transmit 103-bit data using the \( V_{DD2} \) output.

Fig. 5. Simulated transition characteristics of the sub-nanoampere two-stage power management circuit.

3. Experimental Results

To confirm the effectiveness of the proposed circuit techniques, we fabricated a test chip using the 0.35-\( \mu \)m CMOS process. To evaluate the characteristics for the voltage-monitoring circuit, we measured the time for charging the accumulation capacitor with a DC current source. Charging time was obtained from the waveform in Fig. 6. In this measurement, the DC current of 1 nA was input to the rectifier and the voltage (\( V_{DD1} \)) was measured. The accumulation capacitance is 2.2 \( \mu \)F, which is needed to operate our OOK transmitter for one data transmission [5]. The interval of the measured pulse corresponds to charging time, as shown in Fig. 6. The lower waveform shows that the voltage monitor circuit detects the voltage of 1V in accumulated energy. The detected voltage is not the expected value and not high enough to operate the second stage of the power management circuit. This is because the transistor model used for the circuit design could not satisfactorily predict the sub-nanoampere-level current behavior of the voltage monitor circuit.

In Fig. 7, the solid line shows the measured charging time and the dashed line is the calculated one for a reported circuit [7]. For that circuit, the accumulation capacitance cannot be charged when the generated current is less than 0.1 \( \mu \)A. On the other hand, the proposed circuit charges the accumulation capacitor with 1-nA current. Fig. 8 is a microphotograph of the test chip. The chip size is 2 x 2 mm². The power management circuits (excluding the accumulation capacitor) occupy an area of 0.8 x 0.6 mm².

4. Summary

A sub-nanoampere two-stage power management circuit that uses off-chip capacitors for energy accumulation is presented. Focusing on the leakage current and the transition time of the power switch transistor, we estimated the minimum current for accumulating. On the basis of the results, we devised a two-stage power management architecture for sub-nanoampere operation. The simulated and experimental results for the power management circuit describe the operation for a 1-nA current source.

References