Distribution of Characteristic Changes in MOSFETs Induced by Resin-Molded Packaging Stress

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1. Introduction

Recently, state-of-the-art portable electronic devices such as mobile phones have been remarkably improved in terms of compactness and enhanced functions. Due to these improvements, power-management integrated circuits (ICs) require greater accuracy in operation to enable the entire system to be efficiently controlled. One of the main factors that limit the accuracy of ICs is stress-induced performance reduction due to the piezo effect generated during the plastic encapsulation process. This characteristic performance reduction cannot be considered in conventional circuit design if the SPICE model parameter extracted at the wafer stage is used. Consequently, this fluctuation might cause a fatal error in the total circuit performance.

In this paper, packaging-induced performance reductions for a small-scale IC (as typified by power-management ICs) are evaluated using specially designed test chips. A unique experimental method is proposed and distribution charts of stress-induced characteristic changes due to the resin-molded packaging process are presented.

2. Experimental

A. Measurement of packaging-induced stress

To visualize the stress distribution in a small-scale chip with a limited number of bonding pads, specially designed stress sensing test chips and a cantilever bending calibration system have been developed [1]. Both p- and n-type implanted resistors were embedded in the test chip as strain gauges (Fig. 1). Multiple test chips with different resistor locations were measured by die-to-die correspondence between the wafer and the encapsulated stages. Each piezoresistance coefficient was experimentally determined through controlled uniaxial loading using the cantilever system (Fig. 3). A single stress distribution chart was generated from the data for all the test chips (Fig. 2). Fig. 4 shows distribution charts for the y-direction stress (Sy) and the x-direction stress (Sx) components for a 0.8 mm × 1.2 mm test chip.

B. Prediction of stress-induced performance changes

The stress dependencies of transconductance (Gm) changes in long-channel NMOSFET and PMOSFET were measured using this cantilever system. The measurement was performed in such a way that the current flow in the element was parallel and perpendicular to the stress direction. Figs. 5 and 6 show the stress sensitivities of the

MOSFETs. The NMOSFET exhibits shifts in the same direction for both parallel and perpendicular stresses. In contrast, the PMOSFET shows the opposite trend. As shown in Fig. 4, a silicon chip is placed in a state of the biaxial compressive stress field after packaging. Stress-induced Gm changes (ΔGm) in the encapsulated MOSFET are then expressed by the following equations:

$$\Delta Gm = \pi_L Sy + \pi_T Sx \qquad (1)$$

$$\Delta Gm = \pi_T Sy + \pi_L Sx \qquad (2)$$

where π_L and π_T represent the stress sensitivities when the current flow in the MOSFET is parallel and perpendicular to the stress direction, respectively. Equations (1) and (2) show the Gm changes in longitudinally and transversely arranged MOSFETs, respectively (see Fig. 7).

3. Results and Discussion

NMOSFET shows a shift of about –4.0 % over the entire chip area in both longitudinally and transversely arranged MOSFETs (Fig. 7). The larger negative shifts are caused by the additive effect resulting from the biaxial compressive stress. Compared to NMOSFET, PMOSFET exhibits a definite symmetrical distribution around the chip center (Fig. 8). Complicated behavior is observed about the arrangement. A positive shift of approximately 3.0 % is observed in the central area of the chip for a longitudinally arranged MOSFET. In contrast, a transversely arranged MOSFET has a smaller negative shift of approximately –1.0 %. This characteristic of PMOSFETs is a result of the subtractive effect that is due to the complete reversal of the Gm change with stress.

4. Conclusions

The distributions of packaging-induced characteristic changes for MOSFETs were evaluated using the proposed method. The results reveal that not only MOSFET selection but also the orientation should be considered when evaluating packaging-induced performance changes for increasing the precision of ICs.

References

[1] N. Ueda et al., "A Study of Packaging-induced Stress Distribution for Small-scale Silicon Chips," SSDM 2009.
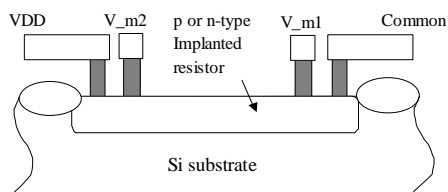
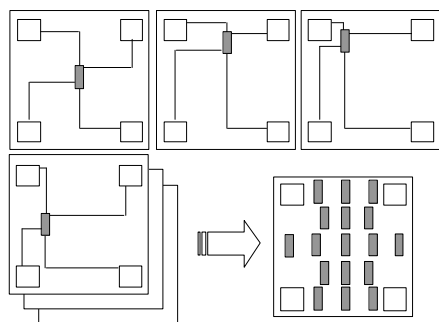Fig. 1. Cross-sectional diagram of piezoresistor.

VDD V_m2 p or n-type Implanted resistor V_m1 Common

Si substrate

Fig. 2 Principle of multiple-point measurements.

Fig. 3 Cantilever bending calibration system.

Parametric Change / Stress

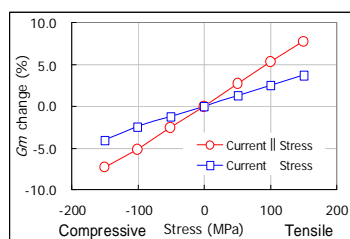Current/Voltage Sources

Load Cell

Environmental Chamber

DUT

Clamp
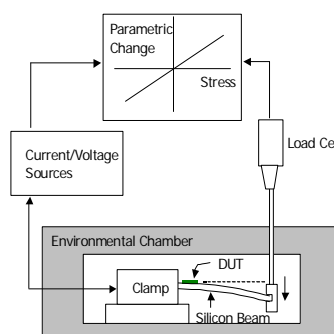
Silicon Beam

Fig. 5 Gm dependence on mechanical stress for NMOSFET.
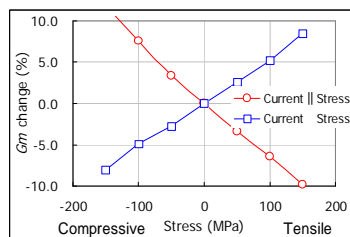
Fig. 6 Gm dependence on mechanical stress for PMOSFET.

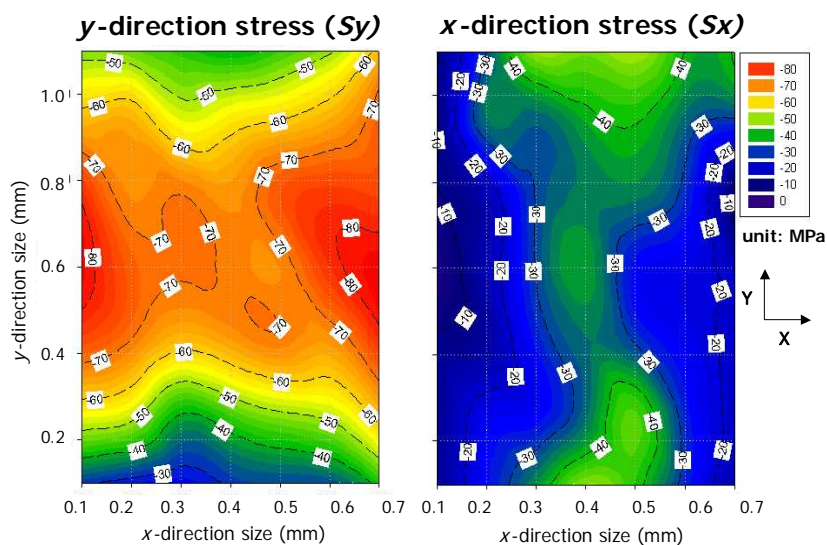**y-direction stress (Sy)**　　**x-direction stress (Sx)**

unit: MPa

Fig. 4 y- and x-direction stress distributions for a 0.8 mm × 1.2 mm Si chip.

Longitudinally arranged NMOSFET　　**Transversely arranged NMOSFET**

unit: %
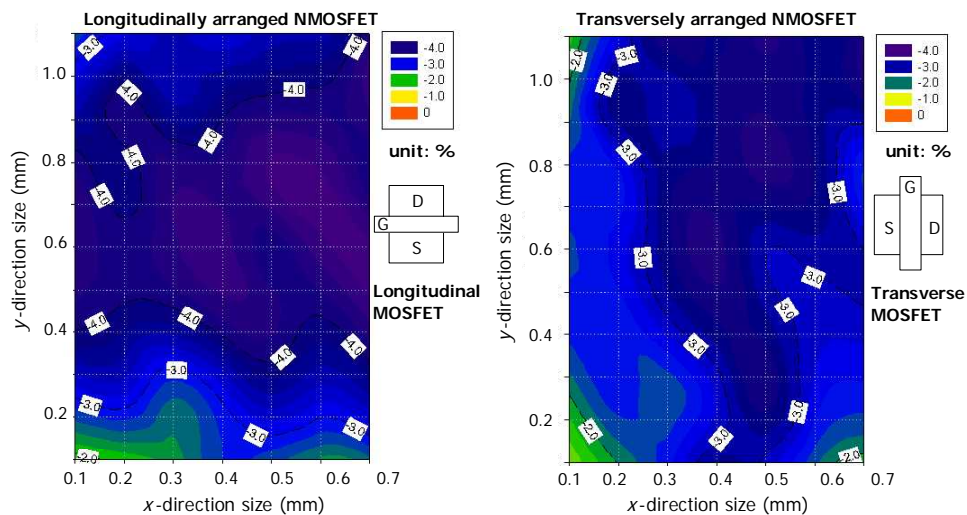
Fig. 7 Stress-induced Gm change distributions for a NMOSFET.

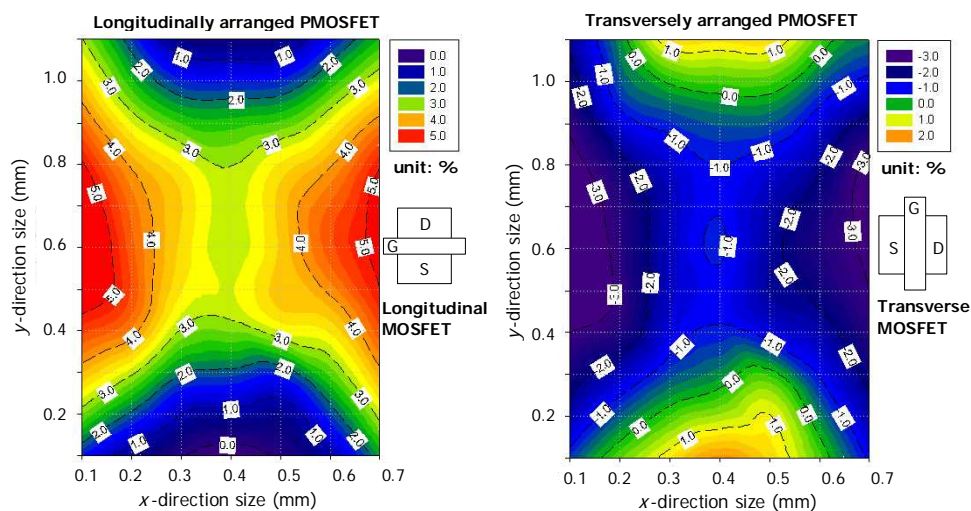**Longitudinally arranged PMOSFET**　　**Transversely arranged PMOSFET**

unit: %

Fig. 8 Stress-induced Gm change distributions for a PMOSFET.