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Low-Voltage and High-Speed Voltage-Controlled Ring Oscillator with Widely Tuning Range in 0.18μm CMOS

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1. Introduction

The voltage-controlled oscillator (VCO) is the most critical component in phase-locked loop (PLL) circuits. Typically, the VCO is built using a ring oscillator or LC resonator in CMOS process. Although the LC resonator has better noise performance and higher operation frequency, the larger on-chip spiral inductor and narrower tuning range are its deficiencies. On the other hand, the ring oscillator can achieve a wide tuning range easily in small chip estate, but it has worse noise performance and lower operation frequency.

The demand for low-voltage operation and high integration has continuously driven the development of the voltage-controlled ring oscillator (VCRO). The source capacitively coupled current amplifier (SC3A) [1] and multiple-pass loops [2, 3] have been proposed to improve the operation frequency and phase noise. However, the control voltage of these VCRO's can not cover the full supply voltage range due to the required turn-on voltage of transistors used in the delay cells, as shown in Fig. 1(a). Besides, the nonlinear voltage-to-frequency characteristic limits the possible highest operation frequency. To overcome the limitations posed by the turn-on voltage, we proposed a complementary control scheme on the delay cell for extending the control voltage range of VCRO to cover the full supply voltage range, as the dash line shown in Fig. 1(b). Consequently, the proposed scheme can also promote both the tuning range and the operation frequency.

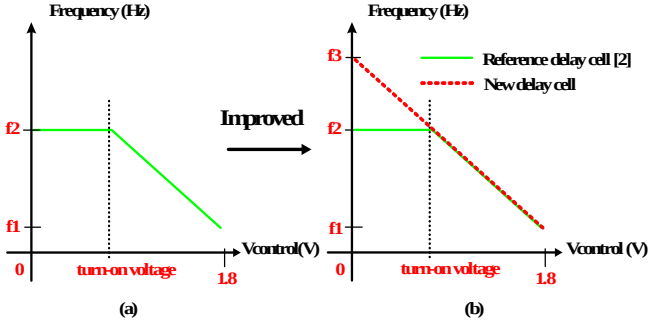

Fig. 1 The idea of the proposed control scheme to extend the control voltage range and operation frequency range.

2. The Complementary Control Delay Cell

The oscillation frequency f_0 of a VCRO is determined by the total propagation delay time of the delay cell, as calculated by $f_0=1/(2NT_d)$, where N is the number of delay stages and T_d is the propagation delay time of the delay cell. Reducing the number of stages [4] and/or the propagation delay time [1-3, 5] are intuitive to enhance the oscillation frequency. However, the frequency control voltage ($V_{control}$) must ensure the turn-on of transistors, or the operation frequency is out of control and also limits the achievable highest operation frequency. In this work, we propose a delay cell with complementary control, as shown in Fig. 2. A pair of PMOS complementary control transistors, M9 and M10, is added to the delay cell for providing an extra current to overcome the limitation of low $V_{control}$ operation as well as to increase the oscillation frequency. The delay cell has a differential structure to reduce the common mode noise. M5 and M6 constitute a latch in the delay cell. The cross-coupled pair, M3 and M4, controls the maximum gate voltages of the PMOS load and adjusts the strength of the added latch and the operation frequency. When $V_{control}$ is less than $V_{gs(4,3)}+V_{ds(1,2)}$, the strength of latches becomes weak, so the complementary control transistors are utilized here to provide the extra current for increasing the operation frequency and the linear controllability of tuning range. The $V_{control}$ controls the delay time by adjusting the loading of M9 and M10. When $V_{control}$ is larger than $V_{gs(4,3)}+V_{ds(1,2)}$, the complementary control transistors become weak, on the contrary, the latch becomes strong and resists the voltage switching in the differential delay cell. As a result, the delay time is increased.

In this paper, the new differential delay cell is verified as employed in a three-stage VCRO utilizing multiple-pass loops structure [2], as shown in Fig. 3, to work at higher operation frequency, increase the tuning range, and reduce the phase noise of the overall VCRO. The VCRO has two operating loops, a primary loop (in solid line) and a secondary loop (in dashed line). P+ and P- are the primary-loop inputs of a delay stage, and S+ and S- are the secondary-loop inputs.

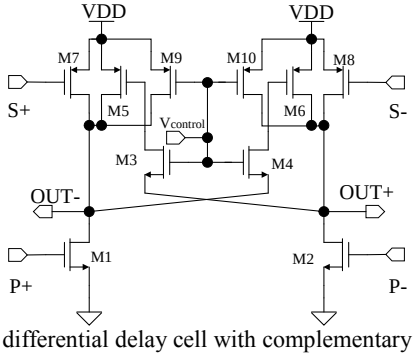

Fig. 2 The differential delay cell with complementary control.

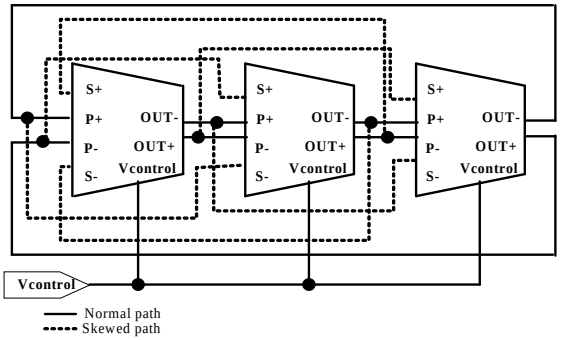

Fig. 3 The three-stage ring oscillator with multiple-pass loops.

3. Experiment Results

The proposed VCRO is implemented in 0.18μm 1P6M CMOS process. Fig. 4 shows the chip photograph. The core area is 106×76.2μm^2. The measurements are performed on-wafer by using Signal Source Parameter Measurement System (includes Agilent E5052A signal source analyzer, E5053A down converter, and E4407B spectrum analyzer). The measured tuning range, as shown in Fig. 5, is from 8.36GHz to 1.29GHz (84% tuning range) for 1.8V power supply, and is from 4.09GHz to 0.479GHz (88% tuning range) for 1V power supply. The measured output spectrum is shown in Fig. 6. The output is at 8.35GHz with signal strength of -7.93dBm at 50Ω load. The phase noise is -105.59dBc/Hz at 1MHz offset from 8.35GHz center frequency, as shown in Fig. 7. The DC current is about 41.25mA at 1.8V power supply voltage.

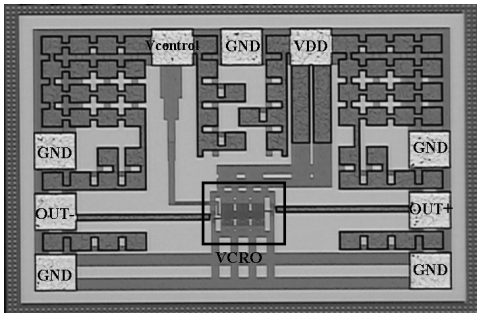

Fig. 4 Chip photograph of the proposed VCRO.

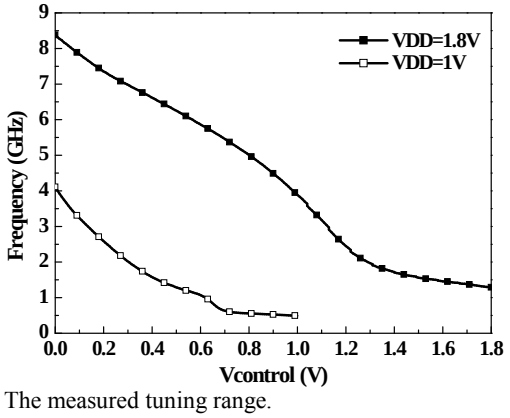

Fig. 5 The measured tuning range.

4. Conclusions

Table I compares the measured performance of our VCRO with other reported works. Our proposed VCRO has full range voltage controllability and achieves a wide tuning range with a best FOM. The full range voltage controllability, favorable for low-voltage operation, is accomplished by employing the proposed complementary control technique in the delay cell.

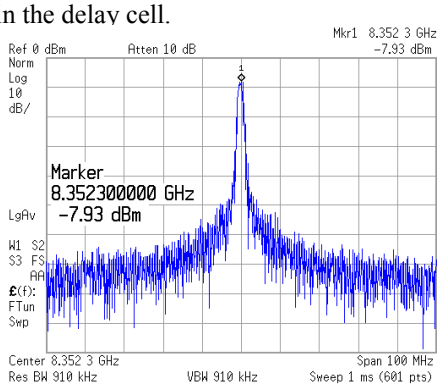

Fig. 6 Measured output spectrum of VCRO.

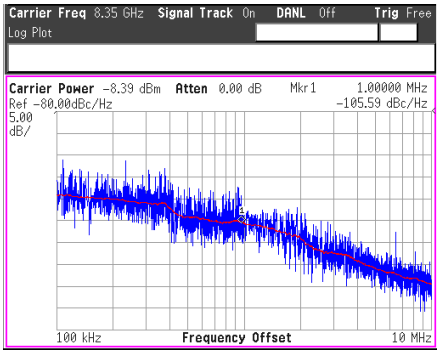

Fig. 7 Measured phase noise of VCRO.

Table I Comparison table with other VCROs

Ref.	[1]	[2]	[3]	[5]	This Work	
Process (μm)	0.12	0.18	0.13	0.18	0.18	
Supply (V)	1.5	1.8	1.5	1	1	1.8
Tuning Range (GHz)	10.6~8.4 20%	5.93~5.16 12.98%	7.86~7.3 7.12%	1.2~0.5 58.33%	4.09~0.479 88.29%	8.36~1.29 84.57%
$V_{control}$ (V)	0.5~1.5	0.3~1.8	0~1.2	0~0.3/0.7~1	0~1	0~1.8
f_0 (GHz)	10	5.79	7.64	1	4.09	8.35
Phase Noise (dBc/Hz)	-85	-99.5	-103.4	-90	-93.3	-105.59
P_{DC} (mW)	52.5	80	91.5	0.71	10	74.25
FOM (dBc/Hz)	-147.8	-155.72	-161.44	-151.48	-155.5	-165.32

* $FOM = L\{f_{offset}\} - 20\log(\frac{f_0}{f_{offset}}) + 10\log(\frac{P_{DC}}{1mW})$ * $L\{f_{offset}\}$: Phase Noise * f_{offset}: 1MHz

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