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A 1 Gb/s Differential Input Threshold Detection Based BPSK Receiver For IR-UWB Communication Using 180 nm CMOS Technology

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1. Introduction

Ultra-wideband (UWB) is a spread spectrum communication system. Three methods are being adopted recently for UWB implementations: direct sequence spread spectrum (DS-SS), multi-band orthogonal frequency division multiplexed (OFDM) and carrier less impulse radio UWB (IR-UWB). The IR-UWB approach, consisting of sending short duration impulses, modulated in time, polarity and amplitude, are well suited for low complexity and low power communications [1]. Gaussian monocycle pulse (GMP) is commonly used for IR-UWB systems [2]. Several receivers are presented in [3] - [5], which depend on coherent detection. As a result, design complexity, price, and power consumption increase. A non-coherent CMOS BPSK receiver employing threshold detection based signal processing scheme is presented in this work. Similar detection scheme has been proposed in [6] but only digital portion has been explained. A complete BPSK receiver in 180 nm process with supply voltage of 1.8 V, capable of retrieving BPSK modulated differential GMP of 1 Gb/s, is described in this work.

2. Operation principle and architecture

The operation principle of the non-coherent differential receiver, along with the detection mechanism, is illustrated in Fig.1. BPSK modulated GMPs are received from antennas and are amplified by the amplifier. The amplified signals are then sent to the detector through the interface circuitry. The detector then retrieves the data from the BPSK modulated signals based on their priority of arrivals. The amplifier, as shown in Fig.2, is a shunt-peaked, 2-stage differential amplifier. The amplifier provides a voltage gain of 15 dB near the center frequency of 3.3 GHz. A DC signal is added to the amplified GMP at the analog to digital interface. While adding the DC, it is made sure that the input MOS device (either MP_1 or MP_2) remains OFF, when no amplified signal is present. In order to accomplish that, the threshold of the interface MOS devices (i.e. MN_1 and MN_2) is kept lower than that of the input devices (MP_1 and MP_2) by making the (W/L) ratio of the former larger than the latter (2 to 1 in this circuit).

The entire detector has been shown in Fig.4. The selector of the detector consists of skewed inverters, where (W/L) of NMOS devices (MP_1 and MP_2) are larger than (12 to 1) that of PMOS devices (ML_1 and ML_2). As a result, the threshold voltage of the NMOS devices is lowered and the selector can respond quickly (typically 150 ps, i.e. the half of the total width of GMP in time domain) to the positive lobes of the GMP templates. The response of the circuit has been shown in Fig.5 (a). The pulses at OP and OM (Fig.4) travel through the RF paths A and B, respectively. The pulse wideners, having self resetting mechanism, enhance the duration of the pulses (at QA and QB) coming from the selector circuit. Pulse widening mechanism is shown in Fig 5 (b). The delay circuits consisting of inverter and nand gates produce the blanking signals BL_A and BL_B. Signals at P_A and P_B are propagating signals through the two RF paths. When the signal arrives at QB earlier (Δt_1) than at QA, the signal at P_B propagates to the latch, whereas when it comes later at QB it is blanked by BL_A. These phenomena are illustrated in Fig. 5(d). This is being called as controlled propagation mechanism 1. Similarly, the controlled propagation mechanism 2 can be explained and it is shown in Fig. 5(e). The latch is either set or reset by the propagating pulses and thus the output is detected.

The chip layout of the receiver has been shown in Fig.6. It occupies a die area of 3.4 mm^2. The extracted netlist has been simulated with a random sequence of data of 1 Gb/s as shown in Fig.7, and it is found that the chip can retrieve data successfully with a power consumption of 76 mW, i.e. it is a 76 pJ/bit receiver. Important characteristics of the receiver have been listed in Table 1.

3. Conclusion

A complete differential input threshold detection based receiver has been demonstrated for the first time. The chip developed in 180 nm CMOS technology, occupying a die area of 3.4 mm^2, can retrieve a BPSK modulated data of 1 Gb/s using a supply voltage of 1.8 V. The receiver, consuming an energy 76 pJ/bit, is suitable for non-coherent (self-synchronized) UWB-IR communication.

References

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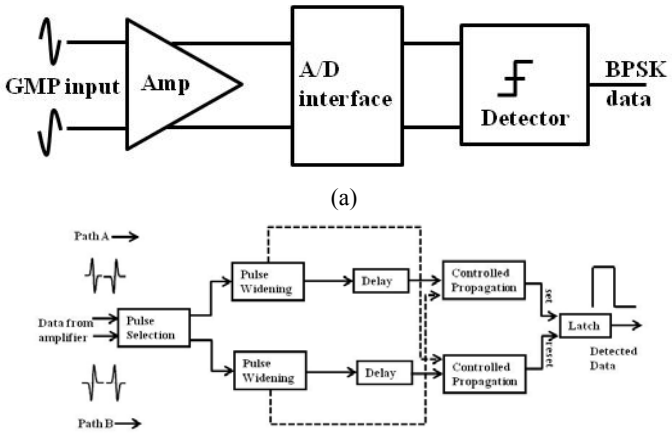


Fig.1. The architecture of the receiver. a). The functional block diagram of the entire receiver. b). The block diagram of the detector.

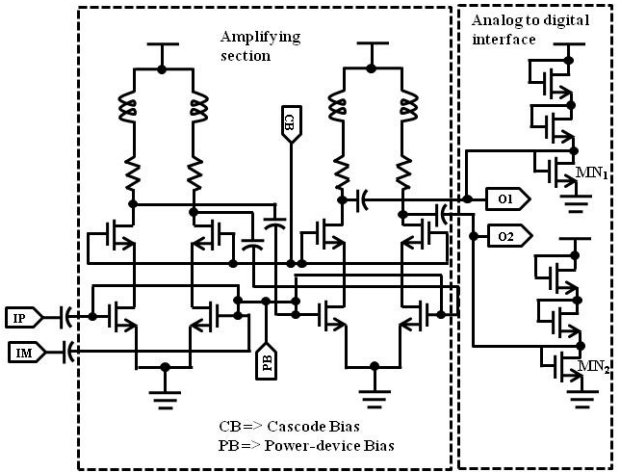
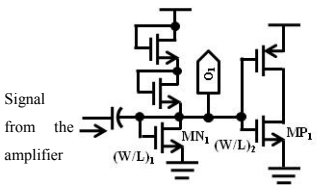


Fig.2. The schematic diagram of the amplifier



$(W/L)_1 > (W/L)_2$
Hence, threshold of MP_1 > threshold of MN_1.

Fig.3. The A/D interface illustrated

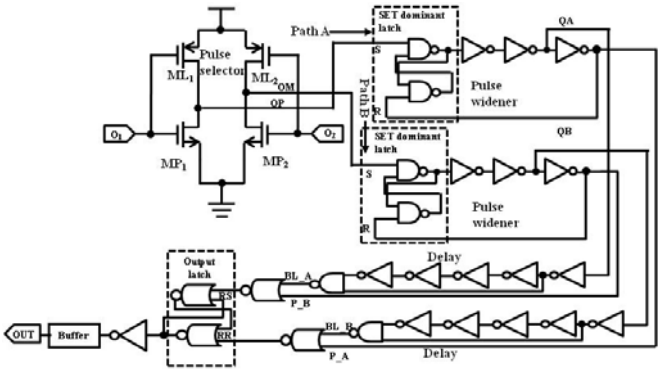


Fig.4. The schematic diagram of the detector

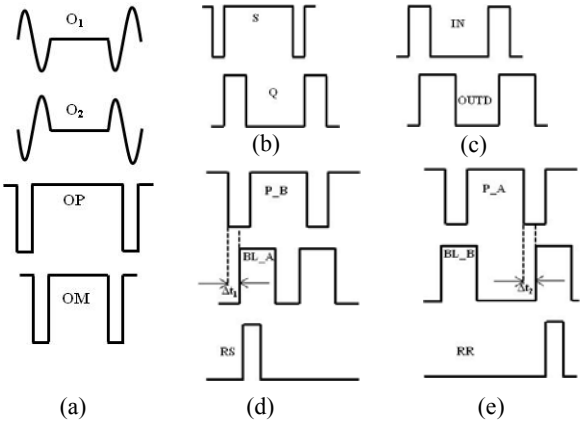


Fig.5. The different functionalities of the detector. a). The pulse selection mechanism. b). The pulse widening mechanism. c). The response of the block delay. d). The controlled propagation mechanism 1. e). The controlled propagation mechanism 2.

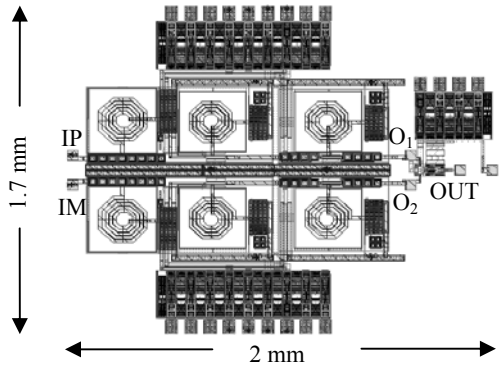


Fig.6. The layout of the receiver

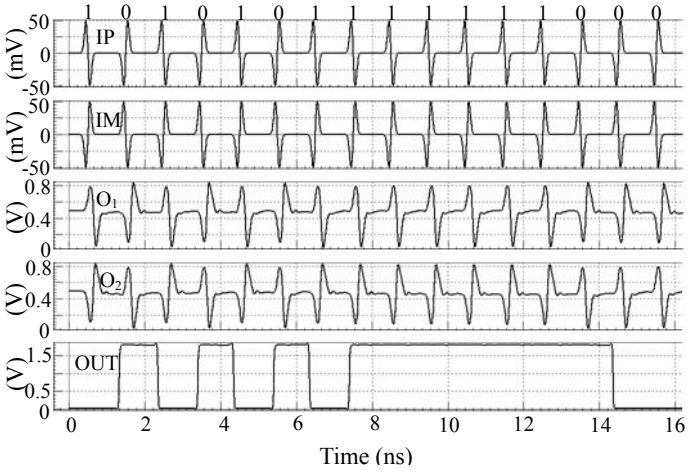


Fig.7. The simulation result of the data recovery by the receiver

Table.1. The important features of the receiver

Technology	180 nm CMOS
Supply voltage	1.8 V
Die area	3.4 mm^2
Data rate	1 Gb/s
Consumed energy	76 pJ/bit
Input mode	Differential
Modulation scheme	BPSK