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A Fractional-N Frequency Synthesizer-Based Multi-standard I/Q Carrier Generation System in 0.13um CMOS

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1. Introduce

In order to reduce the overall terminal mobile phone cost, silicon integration of the multimode transceivers is considered. Nevertheless, this is really cost effective only when transceivers blocks are shared between the different Rx and Tx chains. One of the challenging blocks to design in such transceivers is multi-standard carrier generation system. The frequency synthesizer should enable proper interoperability and seamless connectivity among the various standards considered. Especially, they can generate the in-phase and quardrature(I/Q) waves as LO signals for Zero-IF or Low-IF receivers. Single chip system fully compliant with the IEEE 802.11a/b/g standards was recently presented [1]. It generates two discrete frequency bands with mixers to satisfy the IEEE 802.11a/b/g standards. But it has some spurious tones generated by mixers. Another multimode frequency synthesizer was developed [2]. It used two PLL loops to generate the LO signals, but the frequency band is not continuous. The two carrier generation systems mentioned above can't comply with all standards below 6GHz frequency band.

This paper presents a carrier generation system based on fractional-N frequency synthesizer with three Quadrature VCOs and it generates I/Q LO frequency. The locked frequency range is 2.8~6.1GHz. And successive divide_by _2 prescalers make the frequency from 0.7 to 6.1 GHz continuously by the reasonable frequency planning. Every frequency point has two output paths which is suitable for multi-standard 2×2 MIMO communication applications.

2. Synthesizer Architecture

Fig. 1 shows the architecture of the proposed I/Q carrier generation system. It is the typical fractional-N frequency synthesizer architecture. It consists of a phase frequency detector (PFD), a charge pump (CP) based on switch in source, a presetting module, three quadrature VCOs, a 6bit division ratio extensible programmable multi-module divider, three Mux_Bufs to select the desired QVCO output, successive divide_by_2 prescalers to generate I/Q signals and a digital processor including a 15bit ΣΔ modulator. All components are integrated on single chip except the loop filter (LPF).

3. Switchable Tail Current Source QVCO

Fig. 2 shows the proposed QVCO with switchable tail current source. The complementary CMOS cross-pair topology is used to improve the phase noise performance and reduce the current. Also the switchable tail current source is used instead of constant tail source which can reduce the impact of 1/f noise from the tail current source [3]. According to the SpectreRF simulation result shows in the Fig. 3, the phase noise is improved by 4.5dB at 1MHz compared to the conventional QVCO with the same current consumption.

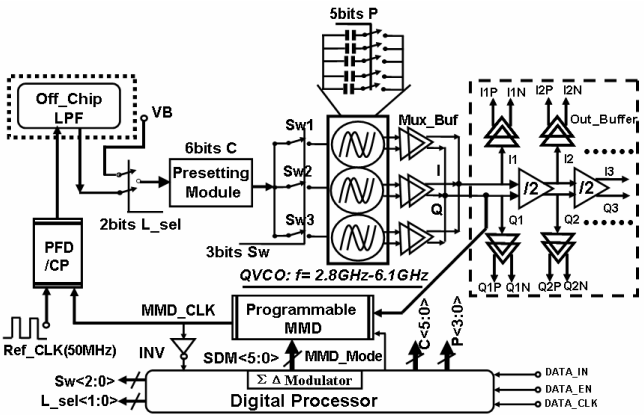

Fig. 1 Architecture of I/Q Carrier Generation System

4. Divide_by_2 Prescaler

Fig. 4 shows Current-Mode logic (CML) static frequency divider that is widely used in high-speed PLLs due to simple design and robust operation. The divider without current source was used that can increase the maximum frequency, reduce power consumption and increase the voltage headroom [4]. The CML divide_by_2 is more ideal than TSPC or ILFD divider below 6GHz frequency operation. The successive divide-by-2 prescalers achieve the frequency from 0.7 to 6.1GHz continuously and generate the I/Q signals.

5. Post Simulation Result

Fig. 5 shows the chip layout with 0.13um RFCMOS process. The total area of the layout is 2mm×1.8mm including all pads. Several post simulations have been done with Cadence SpectreRF. Fig. 6 shows the frequency spans that cover the whole frequency band from 0.7 to 6.1GHz continuously by reasonable frequency planning. The oscillator frequency varies from 2.8 to 4.0GHz in QVCO3, 3.9 to 5.2GHz in QVCO2 and 4.9 to 6.1GHz in QVCO1 respectively. The in-phase and quadrature signals simulated

at 4.86GHz with 50Ω load are depicted in Fig. 7. It can be deduced the amplitude mismatch between the two signals is 1.2%. Fig. 8 shows three QVCOs' phase noise with the different control bits. In the whole band, the phase noise is under -119dB/Hz@1MHz in the worst case. Table I gives the specifics of the chip.

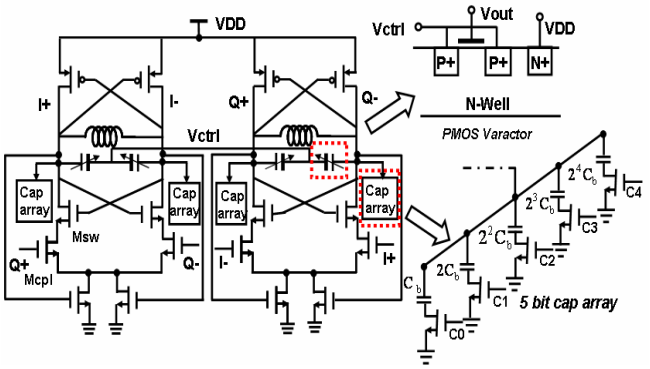

Fig. 2 Proposed QVCO with switchable tail current

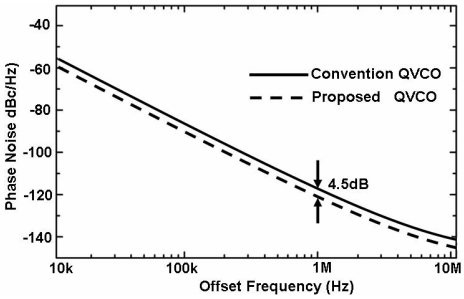

Fig. 3 SpectreRF phase noise simulation for QVCOs

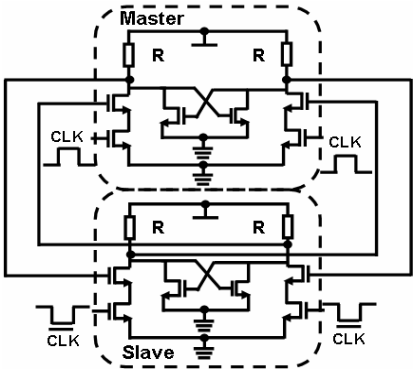

Fig. 4 Divide_by_2 prescaler with CML latch

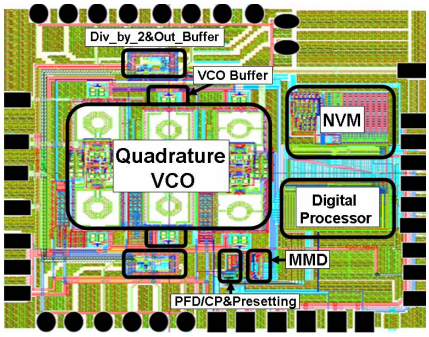

Fig. 5 Layout of the System

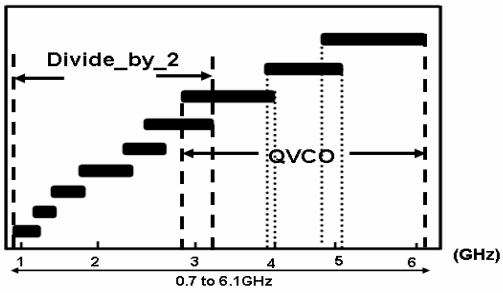

Fig. 6 Frequency plan of the system

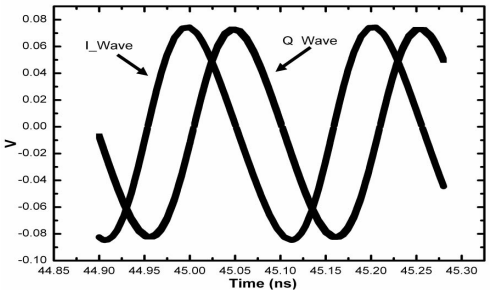

Fig. 7 Output in-phase and quadrature signals at 4.86GHz.

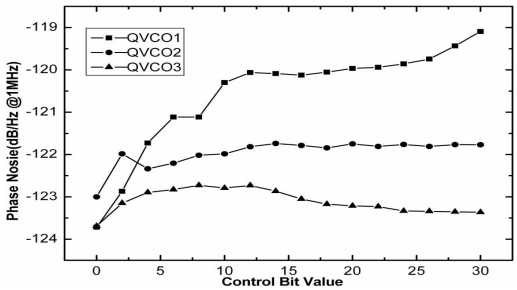

Fig. 8 QVCOs' Phase Noise at the different control bits value

Table I specifics of the proposed chip

Process	0.13um RF CMOS
Reference Clock	50MHz
MMD divide ration	32~127
Frequency range	0.7~6.1GHz(continuously tuning)
Wave type	in-phase and quadrature(I/Q)
Phase Noise(QVCO)	<119dBc/Hz@1MHz(worst case)
Supply Voltage	1.2V
Power	17.5mA(without output buffers)
Area	1.8mm×2mm(include PAD)

References

[1] Z. Xu et al., "A compact dual-band direct-conversion CMOS transceiverfor 802.11a/b/g WLANs," in IEEE ISSCC Dig. Tech. Papers,Feb. 2005, pp. 98–99.

[2] Badets, F.; Camino, L.; Rieubon, S.; Divel, T.; Cerisier, P.; Dedieu, S.; Belot, D, "A Multimode GSM/DCS/WCDMA Double Loop Frequency Synthesizer" Asian Solid-State Circuits Conference,2005, P 201 – 204.

[3] Abumslem Jannesari et "Sinusoidal-switched serial-coupled CMOS LC quadrature VCO" IEICE Electronic Express Vol.4 No.13 426-429 2007 June.

[4] J.Cranickx, "A 1.8-GHz low-phase noise voltage controlled oscillator with prescaler, " IEEE. J Solid-State Circuits, vol.30,no.12 pp 1474-1482, Dec 1995.