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Digitally Controlled Ring Oscillator for Multi-Standard GHz Applications

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1. Introduction

Recently ring oscillator, a crucial part of phase locked loop, has been point of interest for RF communications due to their wide tuning range and compact size. Ring oscillator is advantageous as compared to LC oscillator because of its capabilities to generate quadrature / multiphase output signals without additional circuitry.

Many ring type voltage controlled oscillator (VCO) are designed for high frequency [1]-[5], In these VCO tuning is achieved by varying the supply voltage [1], steering current [2] [5], altering the coupling strength of latch [3]. These methods change the delay of the each stage, and thus, the output frequency is varied. Tuning through variation in supply voltage at low voltages decrease the trans-conductance of gain stages which makes slow transition and increase phase noise. Current steering method of tuning decreases the voltage swing and degrades SNR ratio [4] and altering in coupling strength limits the tuning range and also introduced non-linearity. In Digitally controlled oscillator (DCO] [6] resistance in series with current source is used for tuning which again limits the output amplitude.

All the tuning controlling methods are analog intensive and need large supply voltage, but scaling of CMOS technology and availability of small voltage headroom worsen the frequency control and favors to digital assisted approach. Digitally controlled ring oscillator (DCO) improves the performance and overcome the tuning problem. Digital implementation of ring oscillator in CMOS technology has better compatibility with digital circuits and complete chip can be implemented monolithically.

In this brief we proposed a 9b ring DCO and explored the advantages to use digital control for tuning. The circuit is implemented in 0.18 um CMOS technology and tested.

2. Design of Digitally Controlled Ring Oscillator

High frequency and low phase noise can not be achieved with single loop ring oscillator. So, the DCO is implemented with multiple feed forward architecture [1] in which four inverters (I1-I4) are in main loop and four (F1-F4) in feed forward supporting loop for maximum frequency increase. The block diagram of proposed ring DCO is shown in Fig.1. Inverter of main loop and supporting loop form a single delay cell. The schematic and wiring connection of delay cell is shown in Fig1 (b). PMOS transistors with D0-D8 input are digital control bits. Transistor MP1 and MN1 form the main loop inverter and control slew rate at charging and discharging of output node. MP2 and MN2 are supporting loop inverter and used to avoid latch up.

Current starved method is used for digital implementation. Transistors MC0-MC8 in series with MP1 form the current starved and used for digital tuning. Although, current starved method is not good for tuning because it reduces the output voltage swing. But in digitally controlled it can be used because in digitally controlled method the controlling transistor works in parallel and either they will operate in cutoff region or in deep triode region which reduces the voltage drop across the controlled transistor and output voltage swing is not decreased. Also, we have used 0.1 V higher supply voltage to achieve large voltage swing which increase signal to noise ratio (SNR).

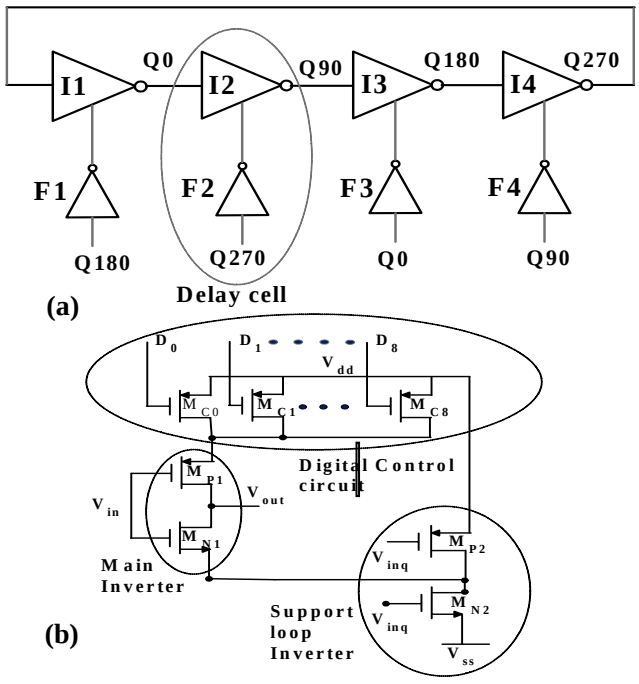

Fig. 1(a) Block diagram of 4 stage DCO. (b) Schematic of delay cell.

The large voltage swing at output node periodically turns on/ off the gain stages, which reduces the noise.. Digital control also makes the circuit robust since the operating region of the control transistors cannot be changed significantly. Power supply fluctuation effect has been minimized deep triode region because of less dependence of current on drain to Source voltage.

The 9b digital control is divided into two parts. Higher order 3b, used to cover the entire tuning range

implemented with PMOS transistors in binary weighted. Also, these 3b compensate the variation in operating frequency due to process, voltage and temperature. Lower order 6b covers one large step with fine tuning step.

The delay of each stage is controlled by the digital control bits in series with the PMOS transistor of main inverter controlling the charging current. Higher the input code higher is the current to charge the output node, higher will be the oscillating frequency.

3. Experiment Results

The proposed 9b ring DCO is designed and implemented in 0.18 um 1P6M CMOS Technology. Chip photograph is shown in Fig.2. The core chip and digital control circuits occupies only 0.09mm^2 excluding bonding pads.

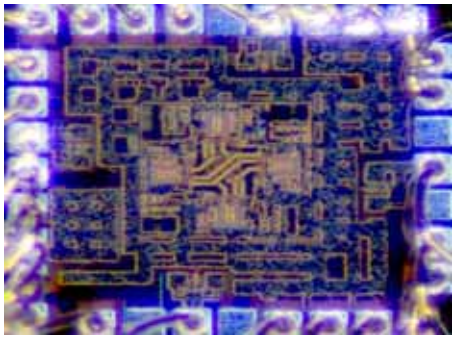

Fig.2. Chip photo of 9b ring DCO.

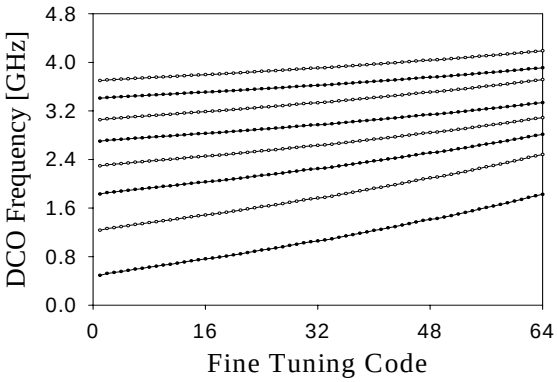

Fig.3. Measured tuning curve for the 9 bit DCO.

The chip is measured using Agilent Signal Source Analyzer (EN5052B). Fig.3 shows the measured tuning range of DCO. Higher order 3b produced different graphs C0-C7, as 6b FTC is varied, that is plotted in x-axis. (C0-C7).The complete tuning range is from 490MHz to 4.2 GHz for the 2V power supply. The measured phase noise is shown in Fig.4. The phase noise is -121.2 dBc/ Hz at 4 MHz frequency offset from 3.86GHz carrier frequency and power dissipation is 48mW. In table I, the performances of the proposed DCO is compared with the other published VCO/DCO where designed DCO shows comparable or better performance with additional advantage of portability to other process.

In [6], tuning control is very complicated which require many switches in series as the number of control bits are increased which is not feasible for multi bit design and may have portability problem although its is a digital design. In our approach tuning bits can be easily added.

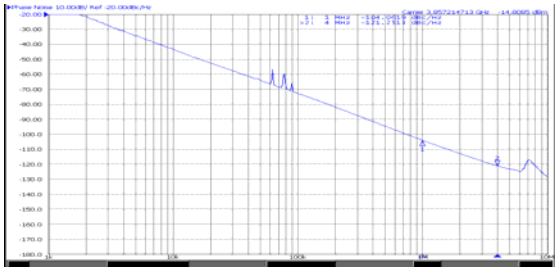

Fig.4. Measured phase noise of proposed DCO at 3.86 GHz oscillating frequency

Table I Comparison of the measured performance

Ref.	$F_{osc.}$ GHz	Power (mW)	PN (dBc)	F_{offset} (MHz)	FOM[1] (dBc)	Tech (um)
[2]	0.1-3.5	16	-106	4	-152.7	0.18
[3]	5.16-5.93	27	-99.5	1	-160.4	0.18
[5]	9.8-11.5	75	-94.0	2	-153.1	0.5
[6]	1.82-10.18	5	-88.4	1	-156.6	0.13
This	0.49-4.2	48	-121.2	4	-164.1	0.18

4. Conclusions

We have designed a 9-bit ring DCO with low phase noise and high operating frequency. The attractive feature is the digitally controlled implementation of ring oscillator design which makes the circuit portable to other process and due to scaling of CMOS technology performance can be significantly improved. Also, fine tuning step can be achieved with large number of digital control bits.

Acknowledgements

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References

[1] O. Nizhnik, R.K.Pokharel, H.kanaya, K.Yoshida, *IEEE Micro. Wire .Compo. Lett.* **19 (**2009) 470

[2] M.Grozing, B. Philip, and M. Berroth, *in proc. 29th Eur. Solid State Circuits Conf.* (2003) 697.

[3] Y.A.Eken and J.P. Uyemura, *IEEEJ Sol. Sta.Cir.* 39 (2004) 230.

[4] L. Dai and R. Harjani, *Kluwer Acad. Publishers* (2003).

[5] J.D.van der Tang, D.Kasperovitz and A. van Roermund, I*EEEJ Sol. Sta. Cir.* **37** (2002) 438

[6] B.Fahs, W.Y.A. Ahmad, P.Gamand, *IEEE Trans. Micro. Theo. and Tech* . **57** (2009) 1074.