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The Effect of Field-Plate Technique on CMOS Ring Oscillator

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1. Introduction

CMOS voltage controlled ring oscillators provide wide tuning range while occupying little chip area. Due to the lack of high Q resonance tank, ring oscillators are inferior to *LC* oscillators in terms of phase noise. Therefore, not much attention has been paid on the phase noise of a ring oscillator. The transistor flicker noise contribution in the phase noise can be very little if the waveform of the oscillator is truly symmetry [1]. However, it is difficult to achieve such waveform, especially for ring oscillators. Therefore, the transistor flicker noise would surely have considerable influence on the phase noise. In this work, MOSFETs with field-plates are used to improve the phase noise of a voltage controlled ring oscillator for the first time.

The field-plate (FP) technique has been applied to LC oscillators for flicker noise suppression [2-3]. However, the results of the previous works leaved us some doubt. First, the authors still adopted standard NMOS as tail current sources which could contribute flicker noise through the AM-to-FM mechanism and should better be removed or implemented by FP-MOSFET if the transistor flicker noise is concerned. Secondly, the phase noise results show more improvement in the far-out region ($1/f^2$ region) rather than in the close-in region ($1/f^3$ region).

In this work, two ring oscillators are respectively implemented with field-plate transistors and standard ones in commercial 0.35-um CMOS technology. The rest of the paper is organized as follows. Sec. II describes the design of the ring oscillator and the structure of the field-plate transistor. Sec. III shows the experimental results. Sec. IV summarizes this work.

2. Field-Plate Transistor

The cross-section view of a MOSFET with a field-plate made from *metal-1* is shown in Fig. 1. The field-plate was placed above the poly gate with a distance of -um from the drain terminal to relax the high electric field under pinch-off conditions. As shown in Fig. 1, the field-plate induces a depletion layer which reduces the effective drain-to-source current density near the substrate surface. Moreover, the carriers can be kept away from the interface between the silicon substrate and the oxide, which would lower the opportunity for the carriers to be captured by the surface traps, and hence the flicker noise of the transistor is minimized.

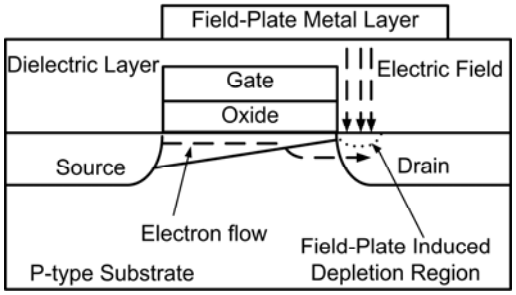

Fig. 1 The cross-section view of a MOSFET with a field-plate made from *metal-1*.

3. Ring Voltage Controlled Oscillator

The schematic of the voltage-controlled ring oscillator (ring-VCO) is shown in Fig. 2. The ring-VCO employs four delay cells, including three inverters and a buffer, to form the basic loop and it offers multi-phase outputs (ex: 0°, 90°, 180°, and 270°).

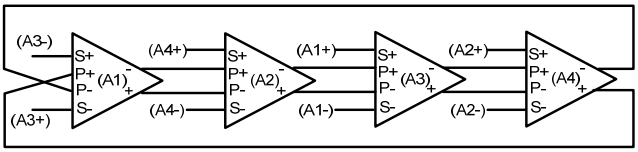

Fig. 2 The schematic of the voltage-controlled ring oscillator.

As shown in Fig. 3 which depicts the schematic of the voltage controlled delay cell, a pair of secondary inputs is adopted to bypass the preceding stage to reduce the effective phase delay contributed by each delay cell to ease the high-frequency operation. Moreover, transistors $M_{1\text{-}2}$ behave as latches, where negative resistance is created to reduce the delay for high frequency operation. Therefore, a wide tuning range can be achieved with transistors $M_{3\text{-}4}$ controlled by the tuning voltage [4].

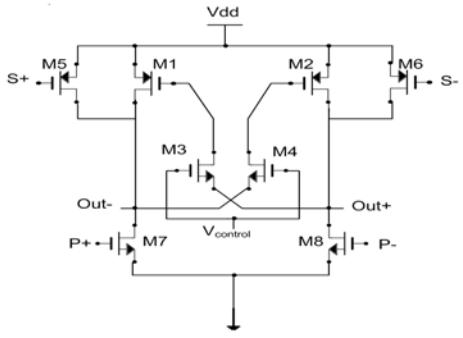

Fig. 3 The schematic of the voltage controlled delay cell.

4. MEASURED RESULTS AND DISCUSSION

Two voltage-controlled ring oscillators (ring-VCOs) were implemented by using 0.35-um CMOS technology. One consists of FP-MOSFETs, called FP-VCO, while the other uses standard MOSFETs, called ST-VCO. The chips were mounted on printed-circuit-boards by wire-bonding for measurement. The measurement was performed with the R&S® signal source analyzer FSUP26. The ring oscillators dissipate 16 mW from 3.3 V. For a controlled voltage from 1.2 to 3.0 V, the measured tuning ranges of the FP-VCO and the ST-VCO are 374~744 MHz and 402~788 MHz, respectively. The slight discrepancy in the frequency range is due to the extra parasitic capacitance contributed by the field-plate [2-3]. To study the influence of the field-plate on the phase noise of a ring oscillator, the phase noise was measured at carrier frequencies of 433 MHz, 470 MHz and 700 MHz, as shown in Fig. 4, where the measurement was repeated twice on two different samples from both FP-VCO chips and ST-VCO chips.

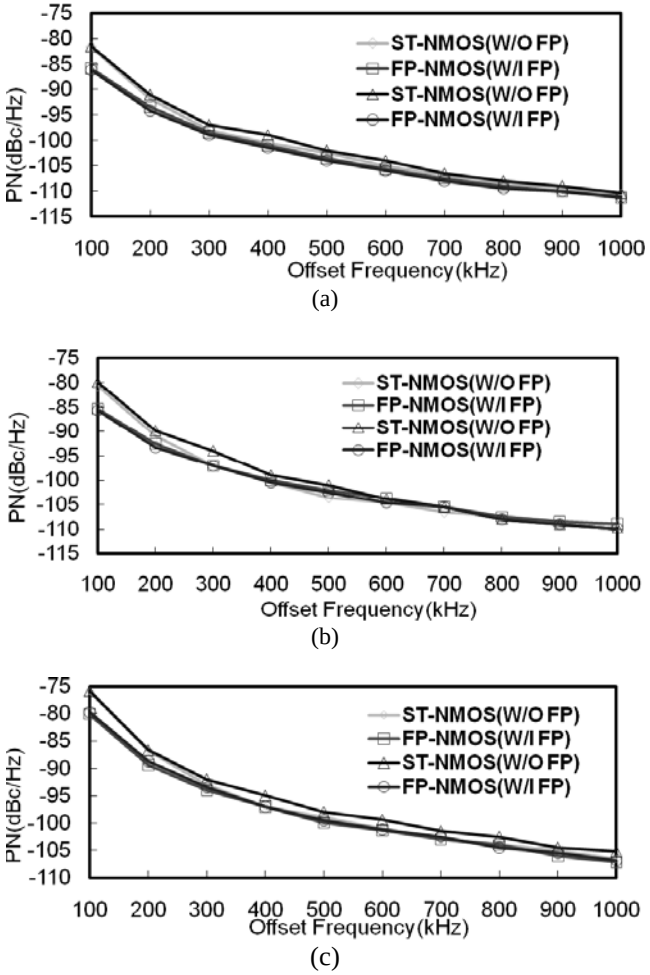

Fig. 4 The measured phase noise results from carrier frequencies of (a) 433 MHz (b) 470 MHz and (c) 700MHz.

Notably, the phase noise curves obtained from ST-VCOs exhibit a slope of -30dB/dec, proving the contribution of the transistor flicker noise. Clearly, the field-plate structure can improve the phase noise at 100 kHz offset by at least 2.5 dB due to the flicker noise suppression. Moreover, the two kinds of oscillators show very little difference in the phase noise at 1 MHz offset, which is predictable since the flicker noise has minor contribution in the $1/f^2$ region.

The microphotography of the ring oscillator is shown in Fig. 5. The circuit occupies a chip area of 0.89 x 0.67 mm^2.

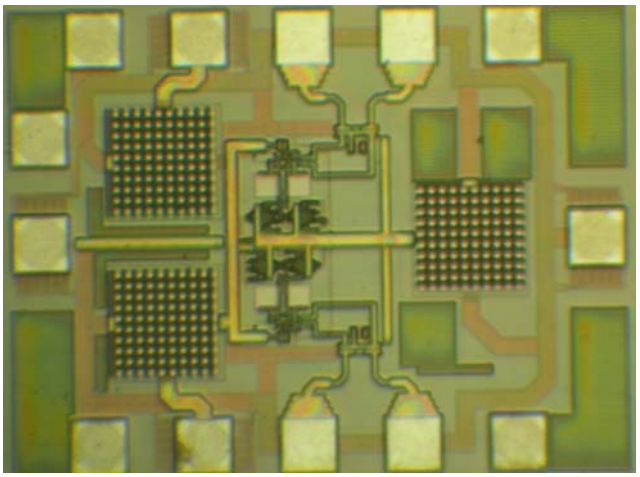

Fig. 5 The microphotography of the ring oscillator.

5. CONCLUSIONS

The transistor flicker noise contributes appreciably in the phase noise of the ring oscillator, even when the tail current source is absent. Moreover, the field-plate technique is proved useful in improving the close-in phase noise of ring oscillators in this work. Since the improvement is mainly due to the flicker noise reduction in the MOSFETs, the technique is less effective in lowering the phase noise in the $1/f^2$ region.

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