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A 12b Two-Stage Single-Slope ADC with Time to Digital Converter

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1. Introduction

A single-slope ADC is the simplest and the smallest ADC and is widely used for column parallel ADC of the CMOS imager. When a ramp signal and an analog one are given to the comparator, the comparator generates a PWM signal. Counting the period of the PWM signal by a clock signal, the analog signal is digitized.

In the single-slope ADC, whenever the accuracy of the ADC doubles, so does the operation time. Therefore, realizing multi-stage ADC by using multi-ramp signal and generating a high-speed-clock signal in the sensor chip has been proposed to solve this problem [1] [2]. In this study, focusing on a quantization error of the single-slope ADC, we developed an effective multi-stage-single-slope one.

2. Structure of proposed ADC

2.1 Operation of proposed circuit

Figure 1 shows a block diagram of the proposed ADC configuration. The ADC has two stages. The first is the 3-bit TDC with multi-phase clock signals, and the second is a 9-bit single-slope ADC with a ripple counter. The comparator of the single-slope ADC generates the quantization error between the outputted PWM signal and the clock signal. The quantization error is given to the TDC, and the error period between the risings of signals is digitized. Therefore, the TDC measures the quantization error of the single-slope ADC (Fig. 2).

2.2 Proposed TDC

Figure 3 shows the proposed TDC configuration. The TDC consists of 4 D-FFs, some logic gates, and a 4-bit ripple counter with a redundant bit for functionality. The proposed TDC uses the special thermo-code. When the master clock period is denoted as T_C, our 3-bit-TDC codes are those given in Fig. 4. The code denotes the time shift of the multi-phase clock. The conventional thermo-code, which is used for the delay-line TDC, is not applied to the proposed circuit. Therefore, considering the 3-bit-resolution, the compact TDC with four D-FFs can be achieved. The proposed circuit has fewer than half the D-FFs the delay-line TDC has. Figure 5 shows the timing chart of the TDC operation. The multi-phase-clock signals *clk_deg0*, *clk_deg45*, *clk_deg90*, *clk_deg135* are given to the input ports of D-FFs. When signal Stop changes, each state of the multi-phase-clock signals is stored in each D-FF. Considering our TDC code, the inverted value of the first D-FF represents the MSB of the 3-bit word, the number of "1" or "0" of the remaining D-FFs indicates lower bits of the 3-bit one. Therefore, using the signals Address [0:3] and cal, we access the D-FFs and update the counter value.

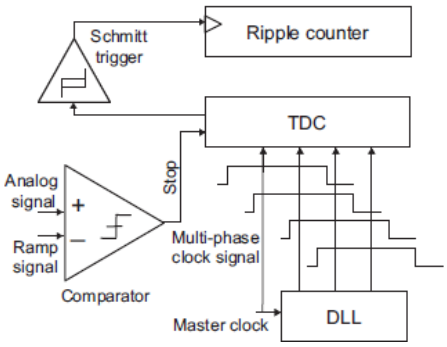

Fig. 1 Block diagram of proposed ADC

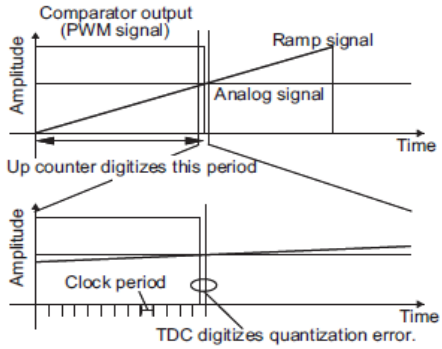

Fig. 2 Operation of proposed ADC

2.3 Consistency of proposed ADC

To achieve the consistency between lower and upper bits in the multi-stage ADC, the master clock *clk_deg0*, which is inputted to the first D-FF of the TDC, is distributed from the D-latch in the D-FF and leads to the LSB D-FF of the ripple counter (in Fig. 1). Moreover, to prevent miscounting to due the D-latch meta-stability, the distributed signal *D-latch_clk* transmits thorough the Schmitt trigger. When the *clk_deg0* value is held as D-latch_clk in the D-latch of the first D-FF, the Schmitt-trigger-output signal *D-latch_clk'* simultaneously stops. At that time, steady-state *D-latch_clk* and *D-latch_clk'* have the same value. Also predefined multi-phase clock *clk_deg0*, *clk_deg45*, *clk_deg90* and *clk_deg135* are provided from the common DLL to the remaining three D-FFs of the TDC. Therefore, the consistency between the first D-FF of the TDC and the LSB D-FF of the ripple counter can be achieved.

A stand-alone single-slope ADC with a delay-line TDC

for low voltage use and a TDC for CMOS imager have been proposed [3][4]. However an additional circuit was required for delay adjustment of the meta-stability. Moreover, since there is no consistency between the stages, digital calibration was also needed.

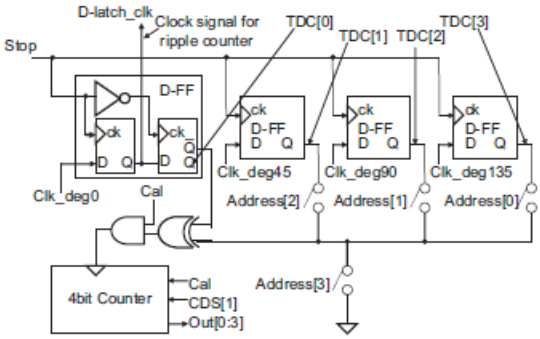

Fig. 3 Operation of proposed ADC

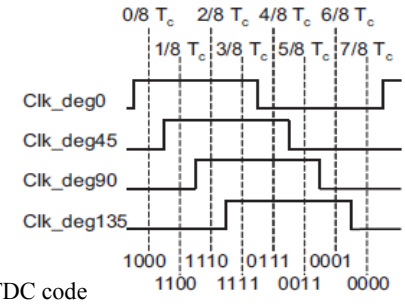

Fig. 4 TDC code

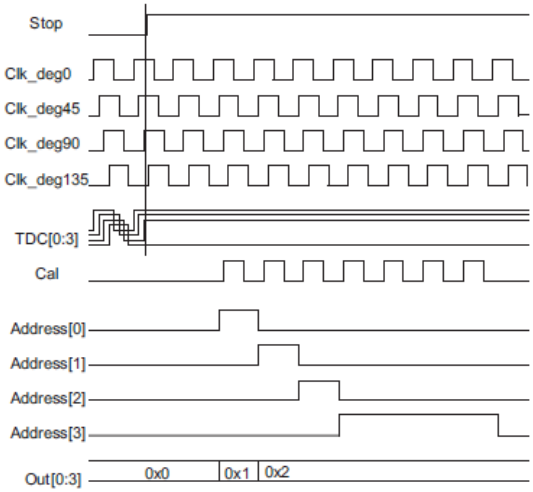

Fig. 5 Timing chart of proposed TDC

3. Simulation results

3.1 Meta-stability analysis

Figure 6 shows circuit delay with the metastability in 0.25μm CMOS process design. The delay time of our circuit was less than 1.6 ns. When the input signal and the stop signal approached, signal distortion was confirmed. It influences miscounting. However, after passing through the Schmitt-trigger, the distortion with half falling and the rising (region of > 4.52 ns) was suppressed because the Schmitt-trigger stabilizes the D-latch output. In our ADC, the simple falling delay (region of =< 4.52 ns) has no effect for the miscounting.

3.2 Linearity of proposed ADC

In the proposed ADC, since predefined multi-phase clocks are used, the clock generator is related to linearity. The comparator delay, clock jitter, signal duty, and process variation of the DLL are key factor. In this study, we also designed a DLL and connected it to the ADC. Considering non-linearity of circuit elements (inc. clock jitter: < 10ps PP, MOSFET mismatch and the comparator delay), simulated DNL and INL of our whole system were ± 0.25 LSB and ± 0.43 LSB @200MHz clock using 0.25μm CMOS process.

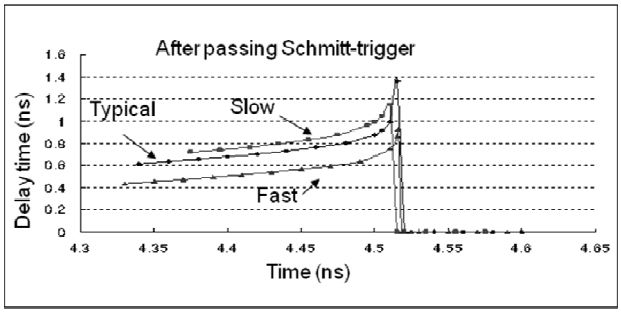

Fig. 6 Circuit delay with meta-stability

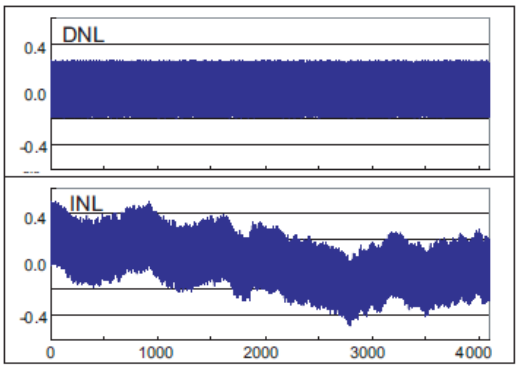

Fig. 7 Linearity of proposed ADC

3. Conclusions

Applying the TDC that uses a multi-phase-clock signal reduced the number of circuit elements, achieved consistency between the single-slope ADC and the TDC, and realized robust meta-stability. We designed a 12-bit ADC, which consists of the 3-bit TDC and the 9-bit-single-slope ADC, by using a 0.25-μm CMOS process.

The quantization errors digitalization was confirmed by Cadence Spectre. Also the meta-stability characteristics and the linearity were analyzed. The operation time of the TDC was less than 5ns for a 200 MHz clock (conversion time: 1.28 us). Therefore, the proposed method is eight times faster than while being as accurate as the conventional single-slope one.

References

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