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A Novel Soft-Start Control Circuit for Current-Mode Buck DC-DC Converters

Kimio SHIBATA and Cong-Kha PHAM
The University of Electro-Communications, 1-5-1 Chofugaoka, Chofu-shi, 182-8585, Japan
Phone: +81-42-443-5165 Email: shibata@vlsilab.ee.uec.ac.jp; pham@ee.uec.ac.jp

I. Introduction

This paper proposes a high speed soft-start control circuit for Current-Mode Buck DC-DC Converters. The proposed control circuit was fabricated in 0.5μm standard CMOS technology. The control circuit achieved the soft start characteristics of 150μs from no load to a maximum load current. It is more than ten times faster than the popular industrial products. The control circuit is not sensitive to the input voltage, operating temperature and inductor value. Analytical modeling, computer simulations, and experimental results on the proposed control circuit confirmed the validity of the proposed design architecture.

II. Proposed Soft-Start Control Circuit

Fig. 1 shows the block diagram of the current-mode DC-DC converter with the proposed high speed soft start circuit. The soft start circuit consists the RAMP generator, the E_{AMP}, the C_{AMP} and two analog sum circuits. The RAMP generator generates the SS_{RAMP}, the $VREF_{RAMP}$, V1, and V2. The SS_{RAMP} is a piecewise linear voltage. The $VREF_{RAMP}$ is a linear ramp voltage.

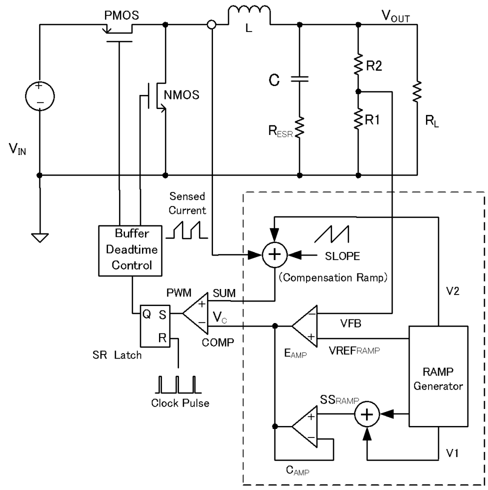

Fig. 1. Block diagram of the current-mode DC-DC buck vonverter with the proposed high speed soft-start circuit.

Fig. 2 shows the Ramp generator circuit. M1 is a variable resistor to generate the $VREF_{RAMP}$. The output of CMP1-CMP3 controls S1-S3 respectively. The voltage which is divided from the VREF by R11-R14 is compared with the $VREF_{RAMP}$ and activates the comparator respectively to increase the charging

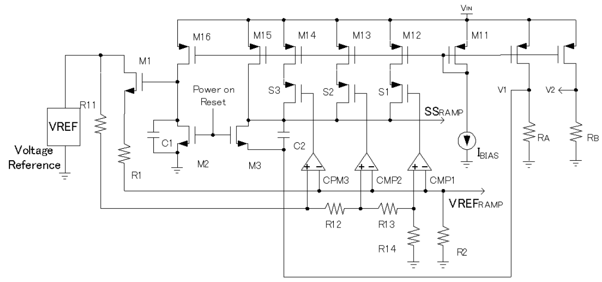

Fig. 2. Ramp generator circuit.

current of C2. The voltage of C2 is the SS_{RAMP} which is a piecewise linear voltage that has four different slopes. The soft-start control circuit operates as follows. (1) The switching is prohibited until the power-on reset signal releases. (2) The PMOS is switched at fixed frequency by a small and fixed duty cycle. (3) The V_{OUT} increase gradually by tracking the $VREF_{RAMP}$. (4) The $VREF_{RAMP}$ is compared with the VREF, and the slope of the SS_{RAMP} increases when the $VREF_{RAMP}$ exceeds 4/10, 5/10, and 7/10 of VREF respectively. (5) The $VREF_{RAMP}$ and the V_{OUT} reach to the equilibrium value. When the peak current of the inductor increases rapidly, the V_{OUT} does not respond to the change of the inductor current. This causes the overshoot output voltage. Thus, the converter requires wideband width for high slew rate. The Slew Rate (SR) is given by [1]

$$SR = (A_{\rm V})(V_{\rm O})(2\pi f_0) \tag{1}$$

The transfer function H(s) of the power stage (L, C, R_L) is given by [2]-[4].

$$H(s) = 1/[1 + (s/\omega Q) + (s^2/\omega^2)] \tag{2}$$

$$f_0 = 1/2\pi\sqrt{LC} \tag{3}$$

The f_0 is the unity gain frequency. The transfer function $T(s)$ of the current-mode converter is givens by [2]-[4].

$$T(s) \quad = \quad T_0 \frac{1+\dfrac{s}{\omega_{\rm z1}}}{1+\dfrac{s}{\omega_{\rm p1}}} \frac{1+\dfrac{\omega_{\rm zc}}{s}}{1+\dfrac{s}{\omega_{\rm p2}}} \frac{1}{1+\dfrac{s}{\omega_{\rm nQn}}+\dfrac{s^2}{\omega_{\rm n}^2}} \tag{4}$$

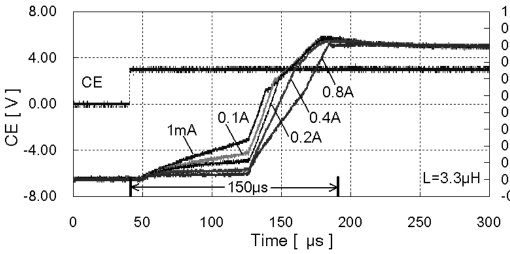

Fig. 3. Soft-Start characteristics of V_{OUT} at I_{OUT}=1mA, 0.1A, 0.2A, 0.4A, and 0.8A. L=3.3μH.

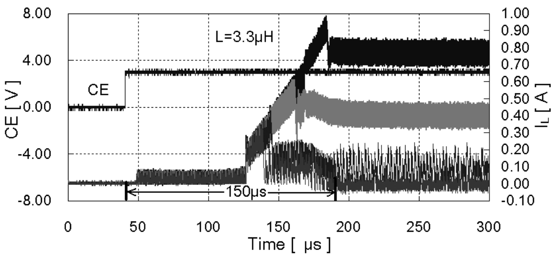

Fig. 4. Soft-Start characteristics of I_L at I_{OUT}=1mA, 0.1A, 0.4A, 0.8A. L=3.3μH.

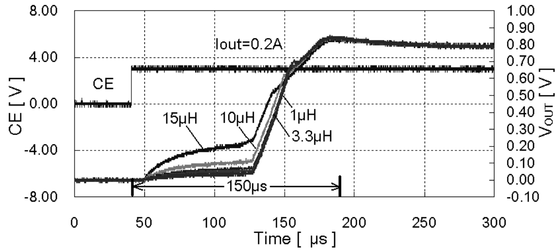

Fig. 5. Soft-Start characteristics of V_{OUT} at I_{OUT}=0.2A, L=1μH, 3.3μH, 10μH and 15μH.

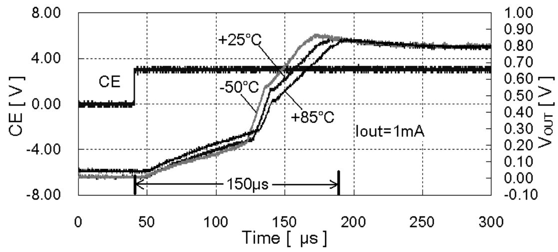

Fig. 6. Soft-Start characteristics of the operating temperature at -50°C, +25°C, and +85°C at I_{OUT}=1mA.

The SR of the SS_{RAMP} increases when the $VREF_{\mathrm{RAMP}}$ exceeds 4/10, 5/10 and 7/10 of the VREF respectively.

1st SR=$2.5m$V/μs, 0V≤ $VREF_{\mathrm{RAMP}}$ ≤0.16V
2nd SR=$5.0m$V/μs, 0.16V≤ $VREF_{\mathrm{RAMP}}$ ≤0.20V
3rd SR=$7.5m$V/μs, 0.20V≤ $VREF_{\mathrm{RAMP}}$ ≤0.28V
4th SR=$12.5m$V/μs, 0.28V≤ $VREF_{\mathrm{RAMP}}$ ≤0.40V

Since the E_{AMP} is clamped to the SS_{RAMP} by the C_{AMP} soon after power up, the V_C is equal to the SS_{RAMP}. At this phase, there is no voltage gain of the E_{AMP} since its output stage is OFF. However, when the E_{AMP} begins linear operation, the V_C is separated from the SSRAMP. Since the DC-DC Converter operates the current-mode. the unity gain frequency f_0 increases. In the proposed circuit, the dc bias V2 and V1 are 400mV and 350mV respectively in order to reduce the soft-start time. A linear ramp voltage of the $VREF_{\mathrm{RAMP}}$ and a piecewise linear voltage of the SS_{RAMP} makes a small differential input voltage for the E_{AMP} during the power up.

III. Measured Results

The measurement result of the DC-DC Converter with the proposed high speed soft-start control circuit is shown in Fig.3 - Fig.6. The proposed circuit has measured at V_{IN}=3.0V, V_{OUT}=0.8V, VREF=0.4V, f_{sw}=1.2MHz. The CE is a chip enable. There was no major influence observed on the soft-start characteristics by entire operating temperature range and input voltage range, and widely selected inductor value. Fig. 7 shows the chip photo and size is is 1.28mm x 1.62mm.

IV. Conclusion

The proposed control circuit has been simulated and implemented in 0.5μm standard CMOS technology. The control circuit achieved the soft start characteristics of 150μs from no load to a maximum load current. The control circuit does not sensitive with the inductor value, the input voltage and the operating temperature. Analytical modeling, computer simulations, and experimental results on the proposed control circuit confirmed the validity of the proposed design architecture. Thus, the proposed high speed soft-start control circuit for implementing to the DC-DC converter will be useful for extending the battery operating time.

References

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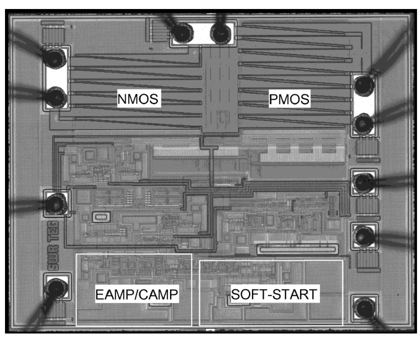

Fig. 7. Chip photograph