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Current stress instability analysis of amorphous InGaZnO thin film transistors

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1. Introduction

Recent researches from the demands of large size liquid crystal flat panel displays, low cost process and higher performance arouse great interest on amorphous oxide semiconductor-based thin-film transistors (TFTs) as an alternative of a-Si TFTs. To achieve device reliability and stability under various current/voltage bias, temperature, and light injections, various researches on amorphous InGaZnO (a-IGZO) channel material have been reported [1,2,3]. It is reported that the deterioration of a-IGZO channel is mainly induced by conditions of trap state, such as oxygen vacancy and it can be enhanced by passivation or annealing process [3]. However, researches on current injection to the TFT channel need to be investigated to achieve optimized performance characteristics at current stress condition. In this study, we investigated channel degradation characteristics applying current stress to a-IGZO channel with different bulk thickness.

2. Fabrication and measurements

For the experiments, the staggered type (bottom gate structure) a-IGZO TFTs fabricated on a glass substrate with 250-nm Mo gate metal deposited by sputtering method were used. 200-nm SiO_xN_y layer was then deposited as a gate dielectric by plasma enhanced chemical vapor deposition (PECVD). The a-IGZO channel was deposited by sputtering method using a polycrystalline $In_2Ga_2ZnO_7$ target with the thickness of 40 nm and 60 nm. The source and drain electrodes were then deposited using sputtering and patterned by photolithography and wet etching. The channel width and length of the TFTs were 200 μm and 50 μm, respectively [4]. Electrical characteristics of the TFTs were measured using a Keithley 236 source measure unit.

3. Results and discussion

The output characteristics with current biased drain voltage were measured repeatedly for 4 times and compared with drain voltage biased output characteristics to investigate effects of charge injection on a-IGZO channel characteristics. The variation of current biased drain voltage characteristics is obvious compared to voltage biased output characteristics for 40-nm channel thickness shown in Fig. 1. The increasing variation at measured voltage over ~6 V or applied current over ~20 μA shows obvious increase of total resistance of channel and source/drain metal/a-IGZO interface. This can be mainly due to the less total net current than injected current from generation/recombination process at the interface of source/drain metal and a-IGZO bulk [5]. Moreover, when the current injection sweep was repeated, the total resistance also increased. The resistance variation is larger at the higher injection current bias condition.

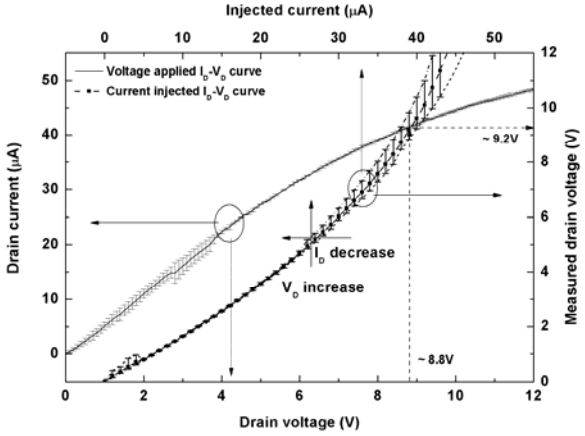

Fig. 1. Comparison between voltage applied I_D-V_D and current injected I_D-V_D curves. (a-IGZO thickness = 40 nm and V_G = 15 V.)

However, in the case of 60-nm channel thickness shown in Fig. 2, previous difference between the transconductance and resistance of output curve and current biased drain voltage curve is relatively small. Additionally, total resistance variation is not correlated to the turns of current bias sweep. Thus, it seems that metal/a-IGZO interface effect is less dominant than 40-nm channel thickness case.

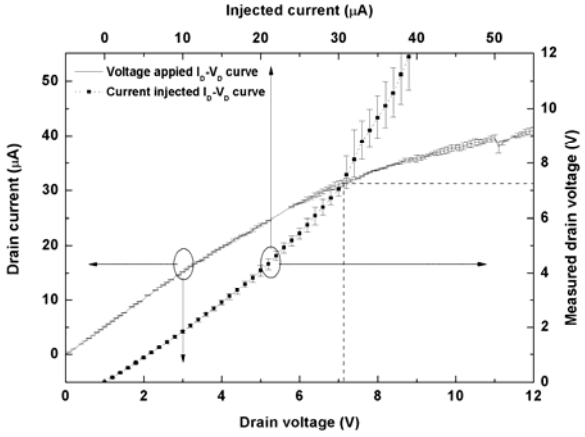

Fig. 2. Comparison between voltage applied I_D-V_D and current injected I_D-V_D curves. (a-IGZO thickness = 60 nm and V_G = 15 V.)

From the previous result, 20-μA constant current stress with gate voltage of 15 V was applied to the test structures for 30 minutes to investigate time dependent channel characteristics variation from injected current stress. Transfer characteristics were measured in every 10 minutes between the current stresses.

The transfer characteristics variation of the TFT for the 40-nm channel thickness is shown in Fig. 3. Transfer characteristics after 4 times of current biased voltage measurement shows subtle increase in threshold voltage. After current stress for 30 minutes, threshold voltage increased. This is related to channel-dielectric interface trap charges [6].

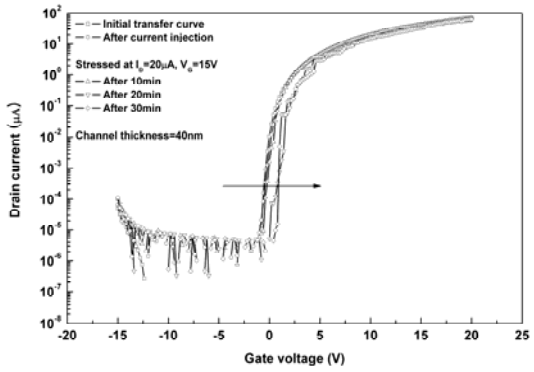

Fig. 3. Transfer characteristics variation for the a-IGZO TFT with 40-nm channel thickness.

For the case of the 60-nm TFT shown in Fig. 4, when the channel bulk thickness increases, threshold voltage shift is also increased since the channel interface charge defects were increased by the injected current [7].

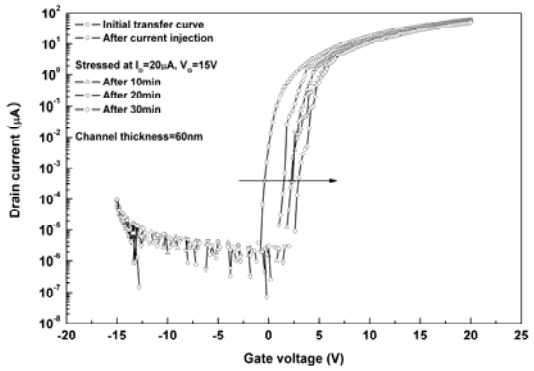

Fig. 4. Transfer characteristics variation for the a-IGZO TFT with 60-nm channel thickness.

From the Figs. 1 and 2, when assuming the S/D resistance of the total resistance is the same which depends on channel width and length, channel resistance of 60-nm thick a-IGZO channel has higher resistance. From this result and the previous transfer characteristic variation, the performance deterioration is larger with the increment of channel thickness when current injection stress is applied. It is due to the relatively higher increase of interface trap charges in the channel and bulk region since the generation and recombination process for the 60-nm bulk thickness case at the metal/a-IGZO interface is less activated than the 40-nm thickness case. It can be originated from either decrease in overlap capacitance due to the increase of bulk thickness or increase of charge conduction probability through the channel bulk based on the hopping mechanism. The verification of the hypothesis mechanisms will be remained as a future work.

3. Conclusions

The electrical characteristic variation of the a-IGZO TFT by current injection stress has been investigated. It was found that the interface characteristics between S/D contact metal and a-IGZO is crucial to achieve stable TFT devices. It is also found the channel thickness of the a-IGZO TFT also a dominant factor to accomplish optimized channel performance based on the results from the successive current biases measurements and current injection stress test.

Acknowledgements

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