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Investigation of Bias Temperature Instability in HfInZnO Thin Film Transistor

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1. Introduction

Recently, oxide Thin Film Transistors (TFT) have received much attention for the future display, mobile electronics and other consumer electronics technology due to its transparency, low manufacturing temperature, high mobility and good uniformity.

HfInZnO (HIZO), in particular, is one of the candidates as oxide TFT's channel material due to its excellent properties. However, its reliability and stability issues have to be solved before it is adopted into the real market, since HIZO's amorphous channel is vulnerable to the stress effect as in the cases of amorphous silicon TFT and other oxide semiconductor materials. [1-3] Therefore, bias stress instability of HIZO TFT has to be addressed.

In this paper, we present the properties and reliability issues in terms of Positive Bias Temperature Instability (PBTI) and Negative Bias Temperature Instability (NBTI). And we analyze the mechanism that causes the instability issues.

2. Experiment

Fig. 1 shows the structure of HIZO transparent oxide TFT used in this experiment. Molybdenum was used as the gate material and it was formed on a glass wafer. Then, the gate dielectric was formed as bi-layer of 400 nm thick SiN_x and 50 nm SiO_2, while SiN_x layer was in contact with gate electrode. After that InZnO with Hf target were co-sputtered for 40 nm thick channel region. Finally, the molybdenum source/drain formation was done, followed by an etching process.

NBTI and PBTI condition is as follows: a constant DC bias was applied to the gate electrode at room temperature, 65 ℃, 85 ℃, 125 ℃. At the same time, source and drain terminals are connected to the ground with the floating body. Then the transfer characteristic was measured with the drain bias of 0.5 V while gate bias sweeping from -15 V to 15 V range.

3. Results and Discussion

Fig. 2 shows a typical transfer characteristic of HIZO at room temperature. The extracted field effect mobility of this device is about 13 $cm^2/V \cdot sec$ and the subthreshold swing is 890 mV/dec. These are remarkable outcomes, compared with the results ever been reported by other groups. [4]

Fig. 3 shows the negative and positive gate bias stress effects of the measured HIZO TFT. As shown in Fig. 3 (a), the negative bias stress effect seems to be negligible in the transfer characteristics. This is due to an extremely low hole density in the channel, since the HIZO TFT is an n-type accumulation mode device. Usually, a TFT is kept in the standby condition affected by the negative bias stress, the NBTI characteristic of HIZO TFT is appropriate for its application. In contrast to NBTI, the transfer curve exhibits a positive parallel shift under the positively biased gate stress, as shown in Fig. 3 (b). In other words, flat-band voltage increases while the subthreshold swing maintains almost the same value. This phenomenon cannot be explained by defect state generation nor removal since it would change the trap capacitance and consequently affects the subthreshold swing. [5, 6]

Fig. 4 shows the threshold voltage as a function of stress time under the positive bias stress condition. The data can be well described by stretched-exponential equation which describes charge trapping induced flat-band voltage change. [7, 8] The stretched-exponential equation is defined as below.

$$|\Delta V_T| = |V_0|^{\alpha}\left[1-\exp\left\{-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right\}\right] \quad (1)$$

$$\tau = \tau_0 \exp\left(\frac{E_a}{\beta k T}\right) \quad (2)$$

V_0 is the potential drop in the insulator and β is the stretched exponential exponent, which is related to the temperature. In our experiment, V_0 is almost the same as $(V_{ST} - V_{T,\,init})$, where V_{ST} is stress voltage and it exhibits no power dependence, i.e. $\alpha = 1$, while the other constants are hardly affected by V_{ST}, as shown in Fig. 5 (a). τ is the time constant for trapping event, which is a function of the thermal activation energy, E_a, that carriers in the channel need to be injected or hop into lower energy states of the insulator. [7] After most of the energy states in the insulator near SiO_2/HIZO interface is filled with electrons from the channel, electrons are emitted from these states and move into the spatially deeper states through the band tail states which could be transport states. [8] The distribution of

trapped charge by this process, leads to the time dependent power law of threshold voltage. [9] The power law component β is roughly proportional to temperature, as shown in the inset of Fig 5(b). The charge injection and change of its distribution yield the increase of the flat-band voltage.

Stressed samples recover about 90 % of its initial state after 24 hours at room temperature without bias stress, as shown in Fig. 6. However the rest of the threshold voltage shift is not fully recovered for a long time. It means that electron trap sites can be divided into deep and shallow states. This result is consistent with trapping process mentioned above.

4. Conclusion

In summary, we have reported some reliability issues on HIZO TFT. Fortunately, HIZO TFT is very stable for negative bias stress, so it will show good reliability under the standby condition. Transfer curves just shift parallel and are well fitted to stretched-exponential equation under positive gate bias stress. It is concluded that electron charge trapping into SiO_2 layer is the dominant mechanism of PBTI.

Acknowledgement

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References

[1] Z. Tang, *et al.*, *Solid-State Elec.*, (2009) 225.
[2] A J Flewitt, *et al.*, *Semicond. Sci. Tech.*, (2009) 7pp.
[3] Jeong-Min Lee, *et al.*, *Appl. Phys. Lett.*, **93** (2008) 093504.
[4] W.H Jeong, *et al.*, *Appl. Phys. Lett.*, **96** (2010) 093503-1
[5] M.J. Powell, *et al.*, *IEEE Trans. Elec. Dev.*, **36** (1989) 2753.
[6] M.J. Powell, *et al.*, *Phys. Rev. Lett.*, **45** (1992) 4160.
[7] F. R. Libsch, *et al.*, *Appl. Phys. Lett.*, **62** (1993)1286.
[8] Don Monroe, *Phys. Rev. Lett*. **54** (1985) 146
[9] T. Tiedje, *et al.*, *Solid State Comm.*, **37** (1980) 49

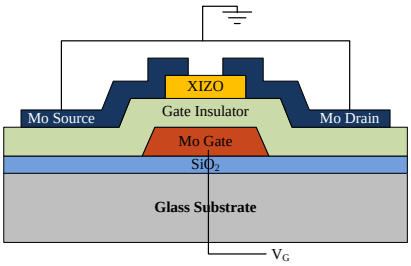


Fig. 1. Horizontal and vertical cross-section of HIZO TFT structure and measuring scheme

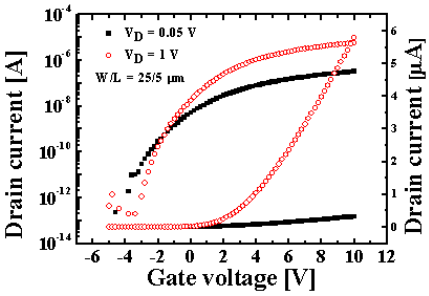
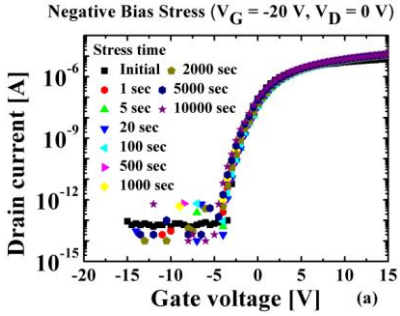


Fig. 2. Positive bias stress effect on the transfer characteristics.



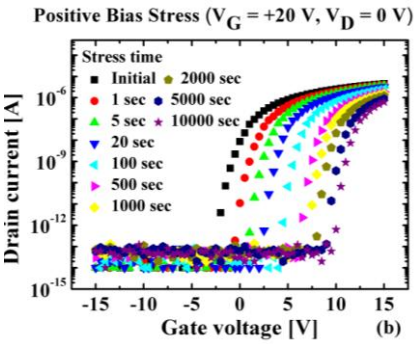


Fig. 3. Bias stress effect on the transfer characteristics.
(a) Negative bias temperature instability
(b) Positive bias temperature instability

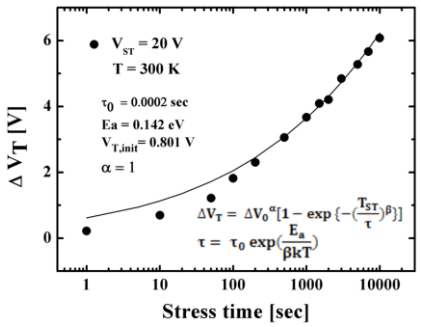


Fig. 4. Threshold voltage shift versus stress time. The symbols represent the measured data and the solid lines are the fit to the stretched exponential equation. The parameters used in the equation are listed on the figure.

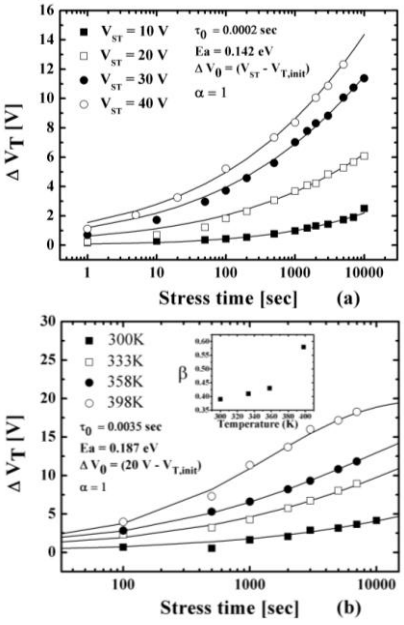


Fig. 5. Threshold voltage shift versus stress time with respect to (a) the stress voltage and (b) the temperature. The symbols represent the measured data and the solid lines are the fitting values to the equation (1), (2).

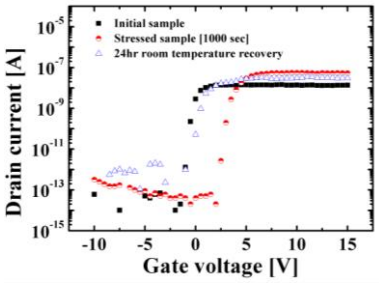


Fig. 6. Transfer curves of initial sample, stressed sample and its recovery after 24 hours at the room temperature.