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Study of the CeO_2/HfO_2/InAs metal-oxide-semiconductor capacitors with different post-deposition-annealing temperatures

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1. Introduction

III-V based metal-oxide-semiconductor field-effect transistors (MOS-FET) have great potential to meet the high performance requirements for due to their high mobility in comparison with silicon. There have been numerous efforts to develop MOS devices on GaAs and InGaAs. However, InAs, known as extremely high mobility and high saturation velocity channel material[1] is probably the best candidate for low power and high speed logic application. But, unlike SiO_2 on Si substrate, there were no stable native dielectrics on III-V compound semiconductor. Various high-k gate dielectrics have been demonstrate on III-V MOSFETs with high drive current density, including MBE growth Ga_2O_3 or Gd_2O_3 on GaAs and InGaAs materials[2]. Recently, HfO_2 with dielectric constant of 25 and energy bandgap of 5.3eV and CeO_2 with high dielectric constant (23–52) and moderate bandgap (3.0–3.6 eV) have attracted a great of interest from industries as the alternative to conventional SiO_2 gate dielectrics[3]. In this work, we investigate the n-InAs with CeO_2/HfO_2 two layers dielectric MOS capacitor to show the better characteristics.

2. Experiment

The device structures of the MOS capacitors under study are shown in Fig. 1. 10nm n-doped $5x10^{17}cm^{-3}$ $In_{0.53}Ga_{0.47}As$, 3nm n-doped $5x10^{17}cm^{-3}$ $In_{0.7}Ga_{0.3}As$ and 5nm n-doped $5x10^{17}cm^{-3}$ InAs were sequentially grown on n^+ InP substrate by molecular beam epitaxy (MBE). High-k dielectric layer of 15nm HfO_2 and 10nm CeO_2/5nm HfO_2 were deposited on n-InAs respectively by MBE to form the MOS capacitors. For HfO_2/InAs device, a 400~550℃ post deposition annealing (PDA) was performed. For CeO_2/HfO_2/InAs device, after RTA annealing, CeO_2 was grown on HfO_2 followed by 400℃ PDA temperature. Finally, W metal was deposited on the dielectric as the gate metal and Au was deposited on the backside of the n+ InP substrate for Ohmic contact for all devices.

3. Results and discussion

Figure 2 shows the C-V characteristics of the CeO_2/HfO_2/InAs MOS capacitor with different HfO_2/InAs PDA temperatures. The capacitors demonstrated strong inversion at 1MHz mainly due to the short lifetime, the higher mobility of the charge in the inversion layer and the high thermal generation rate for InAs material. On the other hand, the C-V characteristics in Figure 2 show the increase of the PDA temperature will increase the capacitance value. However, too higher PDA temperature will cause capacitance value decrease dramatically. The capacitance change varies with PDA temperature can reduce native oxide on HfO_2/InAs interface. However, when PDA temperatures was high than 500℃ the crystallization of HfO_2 will occur which will provide leakage paths and bulk oxide trap charge will increase. Figure 3 shows the CeO_2/HfO_2/InAs C-V characteristics compared with single layer HfO_2/InAs C-V characteristics. The C-V curve demonstrates the high accumulation capacitance value for CeO_2/HfO_2/InAs compared to HfO_2/InAs. The increase capacitance value was due to that CeO_2 has higher dielectric constant than HfO_2. We can also see that the CeO_2/HfO_2/InAs has distinct inversion and accumulation behaviors compare to the HfO_2/InAs. From the C-V curve accumulation region, the EOT value for CeO_2/HfO_2/InAs is 2.5nm and for HfO_2/InAs is 5.6nm. The more than two times capacitance illustrates that combining the higher dielectric constant materials like CeO_2 with HfO_2 can improve the device performance. In addition, figure 4 show the very low leakage current of CeO_2/HfO_2/InAs. This is also an important parameter for MOS devices.

4. Conclusion

We have fabricated CeO_2/HfO_2/InAs two layers high-k dielectric MOS capacitor. The device shows the good C-V characteristics and much higher capacitance value than HfO_2/InAs. It is an attractive candidate for high performance low power logic device applications.

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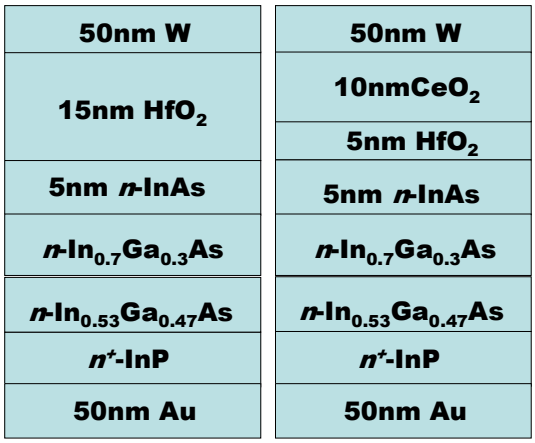

Fig. 1 The device structures of 15nm HfO_2/InAs and 10nm-CeO_2/5nm-HfO_2/InAs capacitors.

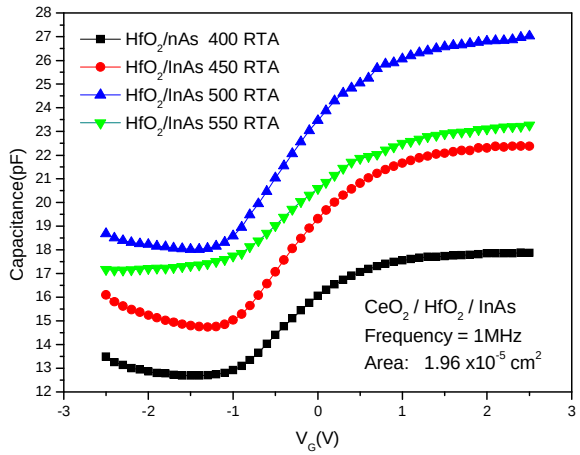

Fig. 2 The C-V characteristics of CeO_2/HfO_2/InAs with different HfO_2/InAs PDA temperatures.

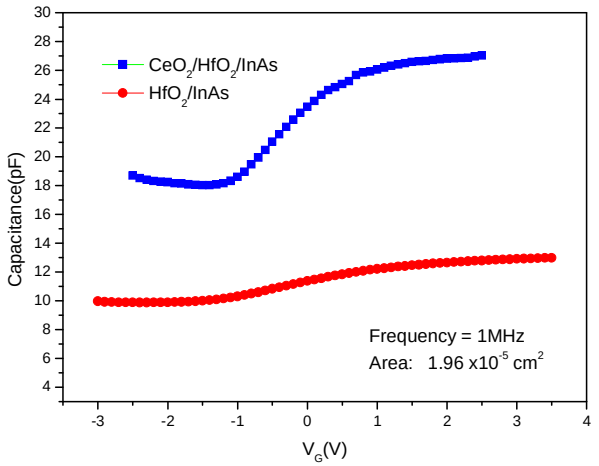

Fig. 3 The C-V curves of CeO_2/HfO_2/InAs and HfO_2/InAs at the same HfO_2/InAs 500℃ PDA temperature.

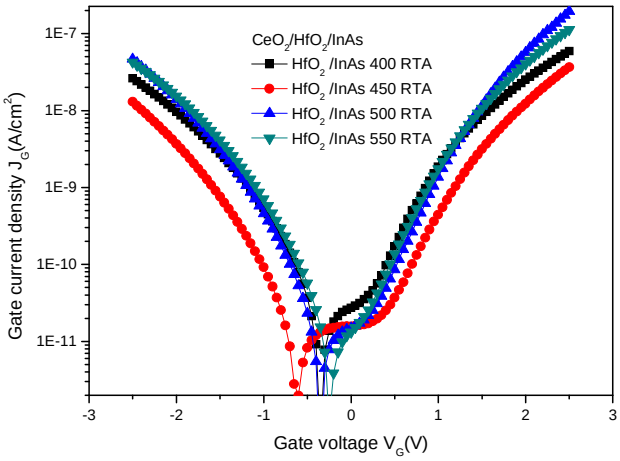

Fig. 4 The gate leakage current of CeO_2/HfO_2/InAs with different HfO_2/InAs PDA temperatures before CeO_2 deposition.