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Short Channel Effect of Indium-Gallium-Zinc-Oxide Thin Film Transistors

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1. Introduction

Thin-film transistors (TFTs) based on hydrogenated amorphous silicon (a-Si:H) or poly crystalline silicon (poly-Si) semiconductor material have been generally used for decades in the flat-panel display (FPD) industry. Recently, oxide semiconductor TFTs have considerable attention in active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) backplane due to high mobility, uniformity and low processing temperature.

Many research groups reported the fabrication of high performance TFTs with Indium-Gallium-Zinc Oxide (IGZO) channel layers deposited by pulsed laser deposition (PLD) and sputter[1-4]. These TFTs showed a high mobility (>10 $cm^2/V\cdot s$) and an excellent subthreshold gate swing (0.20 V/decade) for IGZO TFTs.

However, electrical characteristics of short channel IGZO TFTs still need to be verified to utilize IGZO TFTs as AMLCD or AMOLED backplane. The purpose of our work is to report the characteristics of short channel IGZO TFTs and explain the current conduction mechanism of IGZO TFTs.

2. Experimental Results and Discussion

Device fabrication

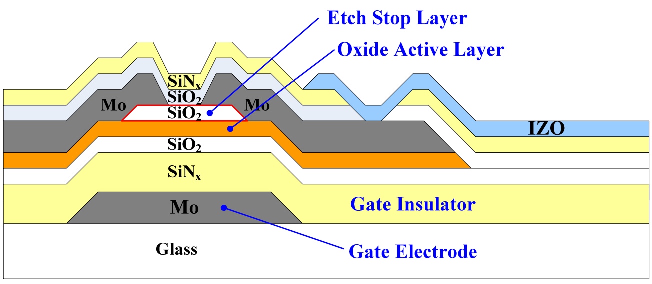


Fig. 1 Cross sectional view of fabricated IGZO TFTs

The IGZO TFTs were fabricated on a glass substrate with a bottom gate structure. Figure 1 shows the cross sectional view of the fabricated IGZO TFTs. First, Mo of 2500Å thickness was deposited and patterned as the gate electrode. SiNx of 4000Å / SiO_2 of 500Å multi-layer were then deposited by PECVD and served as the gate dielectric layer. The IGZO layer with a thickness of 400Å was deposited by sputtering. The SiO_2 etch stop layer (ESL) of 500Å deposited by PECVD. It was used to reduce the damage of active layer during source-drain dry etching process. The source and drain were formed by depositing a layer of Mo and pattered by dry etching. Finally SiNx of 1000Å / SiO_2 of 1000Å multi-layer were used as passivation layer. Channel length can be defined two ways. First way is ELS length, and second way is source-drain metal length. We will specify the channel length both ways.

Electrical characteristics of fabricated device

It is reported that IGZO films exhibit high mobility (10 ~ 20 $cm^2/V\cdot s$) and high carrier concentration (10^{15} ~ 10^{17} cm^{-3}), compared to hydrogenated amorphous silicon[3,4]. So whole active layer can be channel region.

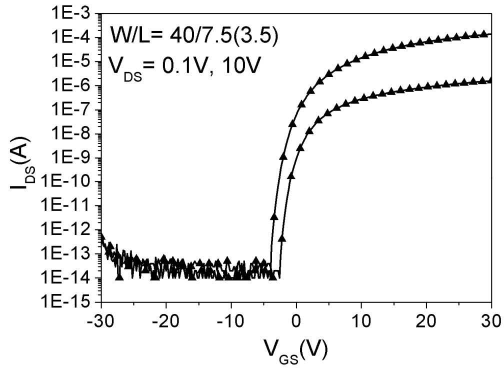
If IGZO TFT have typical electrical characteristics (electron concentration = 10^{15} cm^{-3}, mobility = 10 $cm^2/V\cdot s$) and dimensions (W/L = 100μm/10μm, thickness = 40nm), and apply 0.1V at drain electrode, then the amount of 6 X 10^{-9} A current will flow (from equation (1)). This means that when we design IGZO TFTs, we should consider the whole active layer, not the channel layer near the gate insulator. And we should consider dimension especially active thickness.

$$I = \frac{1}{R}V = \frac{1}{\rho}\cdot\frac{W\cdot t}{L}V = q\mu n\cdot\frac{W\cdot t}{L}V \qquad (1)$$

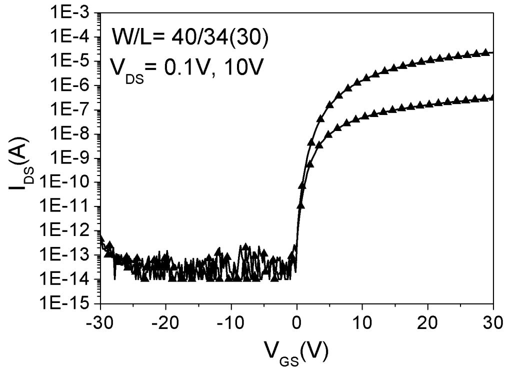
Figure 2 (a) and (b) show transfer characteristics of IGZO TFTs. In Figure 2 (a), in case of short channel length transfer curve certainly shifted to negative direction as much as -1.8 V according to the increase of V_{DS} from 0.1 V to 10 V. On the other hand, in Figure 2 (b), in case of long channel length transfer curve rarely shifted in spite of increasing of V_{DS}.

These phenomena are similar to drain induced barrier lowering (DIBL) in Si devices. As drain voltage is increased, the depletion region of the p-n junction increases in size and extends under the gate. The drain reduces the gate burden, and V_{TH} is negatively shifted.

DIBL effect in IGZO TFTs is some different from that of Si devices. As drain voltage is increased, electric field near drain electrode is increased and electrons are accumulated. These accumulated electrons can act as channel.



(a)



(b)

Fig. 2 Transfer characteristics of IGZO TFTs
(a) short channel device (ELS length = 7.5, S/D length = 3.5μm)
(b) long channel device (ELS length = 34, S/D length = 30μm)

Figure 3 shows the energy band diagram of long channel devices when V_{GS} is applied -2V and V_{DS} is applied 0.1V (red line) and 10V (blue line). L_{total} means total channel length, $L_{effective}$ means effective channel length, and $L_{electron}$ means channel length which electrons are accumulated due to drain bias. The electron quasi-fermi level (E_{Fn}) is lowered at $L_{effective}$, due to negative gate bias.

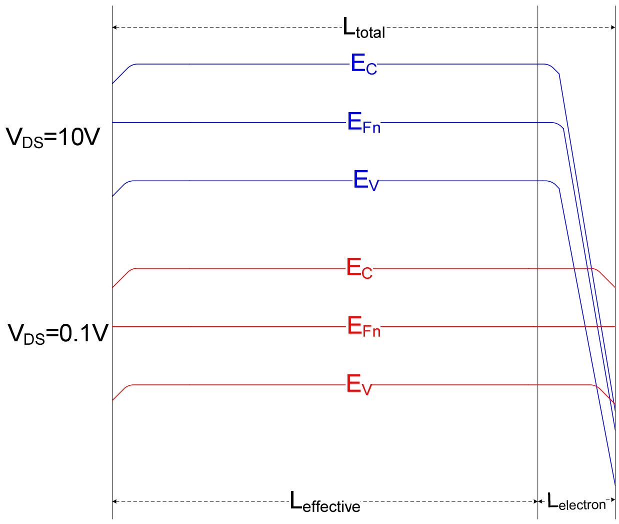


Fig. 3 Energy band diagram of long channel devices

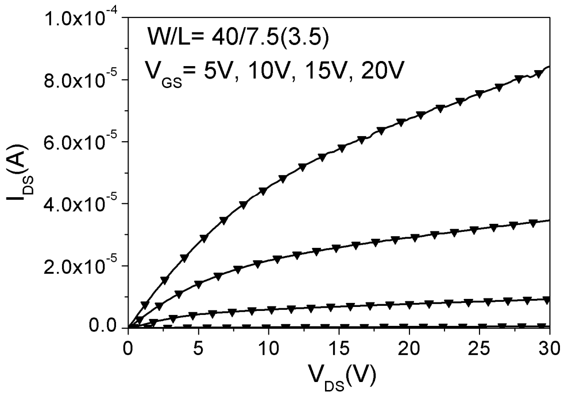


Fig. 4 Output curve of short channel IGZO TFT

$L_{electron}$ can be calculated roughly by equation 2. When V_{DS} is 0.1V, $L_{electron}$ is approximately 0.2 μm. So, it can be ignored at both long channel and short channel device. But, when V_{DS} is 10V, $L_{electron}$ is approximately 2 μm. Thus, long channel device can ignore $L_{electron}$, but short channel device cannot ignore $L_{electron}$.

$$L_{electron} = \sqrt{\frac{\varepsilon_{IGZO}}{qn_{IGZO}} \cdot V_{DS}} \qquad (2)$$

Figure 4 shows output curve of short channel IGZO TFT. Output curve is not saturated, because $L_{electron}$ is large portion of L_{total} in short channel device.

3. Conclusions

We have fabricated and investigated short channel IGZO TFTs. And we have investigated the current conduction mechanism of IGZO TFTs. When we design IGZO TFTs, we should consider the whole active layer, because IGZO films have high mobility and high carrier concentration. As channel length is shortened, $L_{electron}$ portion of whole active layer is increased and short channel effect is appeared.

References

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