# Physics-Based Modeling and Analysis of Compound Semiconductor Devices and Circuits in Extreme Environments

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# 1. Introduction

Advanced electronic devices and ICs based on compound semiconductors, including III-V and SiGe technologies, can offer significant advantages over traditional silicon based technologies in regard to very high speed signal processing and communications [1]. The modern, silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) are capable of extremely high frequency operation, exhibit very low broadband and 1/f noise, and high transconductance per unit area, all at very modest lithographic nodes, making them near-ideal devices for high-speed, mixed-signal circuits [2]. SiGe BiCMOS is also rapidly evolving as a key technology enabler for space and extreme environment electronics, as a result of its built-in total ionizing dose tolerance, enhanced performance at cryogenic temperatures, high-level integration capability, and low cost [3]. However, single event effect (SEE) mitigation in SiGe HBT devices and circuits continues to be an active research area [4-6]. Similarly, the low power and high speed make many III-V devices ideal for satellite applications where space radiation is high. However, the sensitivity of III-V technologies to radiation effects and lack of suitable radiation effects models and analyses has impacted their use in space applications. Thus, the development of radiation effects models, efficient transient simulation capability, and development of radiation hardening techniques are critical to the introduction of these technologies into satellite systems, space-based communications, remote earth sensing arrays, and micro-air vehicles.

To enable better characterization of single-event effects (SEEs) in latest SiGe and III-V technologies, we have enhanced the CFDRC's NanoTCAD 3D/Mixed-Mode simulator [6-9], with new, physics-based models and tools (e.g., hetero-barrier tunneling, accurate Schottky models). Additionally, the NanoTCAD new interface to Geant4 radiation

models with nuclear reactions [10] and the 3D solver capability to model very low temperature behavior [6], enable comprehensive and accurate modeling of radiation effects in nano-scale systems, in the extreme radiation and temperature environments of space. Our unique mixed-mode tool (*MixCad*), coupling the NanoTCAD 3D device simulator with the Cadence Spectre circuit simulator [11] enables direct use of real circuit designs and compact models from the foundry process design kit (PDK). Recent MixCad simulations of SEEs affecting high-speed SiGe HBT mixed-signal circuits matched experimental data well [6], [9]. The new modeling capabilities enable simulation-based development of radiation mitigation techniques for SiGe, III-V and other compound technologies.

## 2. Mixed-Mode Simulations of SEEs in III-V HEMTs

Our modeling and simulation of III-V high electron mobility transistors (HEMTs) has been done in collaboration with the US Naval Research Laboratory (NRL) where extensive experimental studies of radiation effects were done [12, 13]. For this work, NRL provided details of an InP-based HEMT experimental device (geometry, dimensions, layers, materials, doping, etc.) [14] which allowed us to build an accurate, physics-based 3D model of the HEMT for subsequent transient SEE simulations (Fig. 1).





Fig. 1. Schematic cross-section of the analyzed InP-based InAlAs/InGaAs HEMT (S: source, G: gate, D: drain), and our 3D model in NanoTCAD.



#### 3. Modeling of SEEs in Multi-GHz SiGe HBT Circuits

Our new mixed-mode tools were also tested and demonstrated on SEE analysis in a Band Pass Delta-Sigma Analog-to-Digital Converters (ADCs), developed by Northrop Grumman Corporation (NGC). The circuits were tested earlier for SEE response, in particular, for bit error rates introduced by radiation single events. They were designed and fabricated in the IBM 8HP (130-nm) SiGe process. We focused our analysis on a 7.2 GHz npn-HBT based latching comparator subcircuit of the ADC.

We built a full mixed-mode model of the comparator, which included a circuit netlist coupled with a 3D model of selected HBT (Fig. 3) simulated by the CFDRC NanoT-CAD physics-based device simulator [8]. The interface with Cadence Spectre enabled direct simulations of the real circuits, designs, and models from the NGC designers.



Fig. 3. Mixed-Mode simulation setup of the SiGe HBT-based subcircuit for single-event effect (SEE) analysis: the 3D NanoTCAD model with physics-based modeling of Radiation Event (an ionizing track, or imported Geant4 tracks) is coupled with a circuit solver (Spice or Cadence Spectre).

The goal of our mixed-mode simulations was to compute single-event upsets (SEUs), that is, flipped bits at the digital output, driven by the comparator circuit output signal (Vo+ -Vo-). For a sinusoidal input signal of frequency 3.6 GHz, and the clock frequency 7.2 GHz, the expected digital output bit pattern was 1010101..... Fig. 4 shows example computed waveforms of selected important (differential) signals of the comparator circuit: input signal (Vin+ - Vin-), clock signal (Vckp - Vckn), and output signal (Vo+ -Vo-).



Fig. 4. Mixed-mode simulation of the 7.2GHz comparator circuit for an ion strike (LET = 12 MeV-cm<sup>2</sup>/mg) into Emitter of the Transistor 4A. The digital output signal (Vo+ - Vo-) - red line vs. black line/No Radiation - is clearly disturbed: the first two '1' bits are flipped to '0'.

The reference "No-Radiation" results were compared with our simulations of ion strikes of various linear energy transfer (LET) values into the HBT transistors 4A and 4B. The digital output results (Fig. 5) matched the SEE experimental data quite well, and confirmed the validity of our approach and tools.

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MIXED-MODE SEU RESULTS FOR ION IN TRANSISTOR 4A								

Radiation Output Bit Pattern								Comments	
No Rad.	1	0	1	0	1	0	1	0	Expected output
TEL = 8	1	0	1	0	1	0	1	0	No bits flipped
LET = 10	1	0	0	0	1	0	1	0	<b>One</b> bit flipped: $1 \rightarrow 0$
LET = 12	0	0	0	0	1	0	1	0	<b>Two</b> bits flipped: $1 \rightarrow 0$
LET = 14	0	0	0	0	0	0	1	0	<b>Three</b> bits flipped: $1 \rightarrow 0$

Fig. 5. Mixed-mode computed digital outputs of the 7.2GHz comparator circuit, for ion strikes of various LET values (in MeV-cm<sup>2</sup>/mg) into Emitter of the Transistor 4A. The computed results match the measured SEE data quite well.