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Enhanced Light Output of Vertical GaN-Based LEDs with Surface Roughening Using Size-Controllable SiO_2 Nanotube Arrays

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1. Introduction

Recently, many attempts have been made to develop high-efficiency and high-power GaN-based light-emitting diodes (LEDs) for applications of backlight, traffic display, and even solid-state lighting [1-2]. Efforts to enhance the light extraction efficiency of conventional GaN-based LEDs, by means of vertical-conducting structure LED (VLED) and surface texturing or roughening have been reported [3-4]. In essential, a roughened surface could interfere with the total-internal-reflection effect and facilitate photons to find the escape cone for extraction from the LED device. Over the past years, superior improvements in LED efficiency via surface nano-roughening by heteroepitaxially grown ZnO nanowire (ZnO-NW) arrays on GaN top-layer [5-6] have been successfully demonstrated. Nevertheless, the defective in the transmittance of ZnO-NWs impedes the light extraction, being mainly attributed to the relatively low energy band-gap (3.3~3.7 eV) [7]. In this study, to further improve the light transmittance and light extraction efficiency of VLEDs, an efficient n-GaN surface roughening technology using highly transparent SiO_2 nanotube (NT) arrays is proposed and discussed.

2. Experiments

Figure 1 illustrates fabrication process of the proposed VLED with SiO_2 NT arrays (named as SiO_2-NT VLED). After wafer cleaning, annealed-Pt/Al/Pt and Cr/Ti/Au metal systems as highly reflective ohmic contact layer and adhesive layer, respectively, were deposited on p-GaN layer by E-beam evaporator sequentially (Fig. 1(a)). Then, an 80-μm-thick nickel substrate was formed by electroplating and the laser lift-off process was performed at a reactive energy of 850 mJ/cm^2 (Fig. 1(b)) [8]. After the removal of the sapphire substrate, the exposed buffer layer was removed by the inductively coupled plasma (ICP) dry-etching system (Fig. 1(c)). For device isolation, an additional ICP dry-etching was performed to etch epitaxial structure all the way down to the nickel substrate with SiO_2 mask, having device size of 1 mm×1 mm and cutting-way width of 90 μm (Fig. 1(d)). It was followed by the growth of well-ordered and vertically-aligned hexagonal ZnO-NWs on the samples by hydrothermal growth (HTG) method (Fig. 1(e)) [9]. After that, the ZnO-NWs were used as templates for SiO_2 deposition using a PECVD system and subsequently loaded into an ICP chamber to go through a SiO_2 dry-etching to unveil the ZnO-NWs (Fig. 1(f)). The samples were then placed in a chemical solution of H_3PO_4:HCl:H_2O (1:1:10) to remove ZnO-NWs selectively and vertically-aligned SiO_2-NT arrays were obtained (Fig. 1(g)). Finally, a passivation layer and a metal pad of Cr/Al/Cr/Au were deposited on the exposed n-GaN layer (Fig. 1(h)). For comparison and investigation on the contributing factors from the use of SiO_2-NT arrays, VLEDs with ZnO-NW arrays (named as ZnO-NW VLED), VLEDs with SiO_2 coated ZnO-NW arrays (named as ZnO-NW/SiO_2 VLED), and VLEDs without any nano-structure on the surface (named as regular VLED) were also prepared.

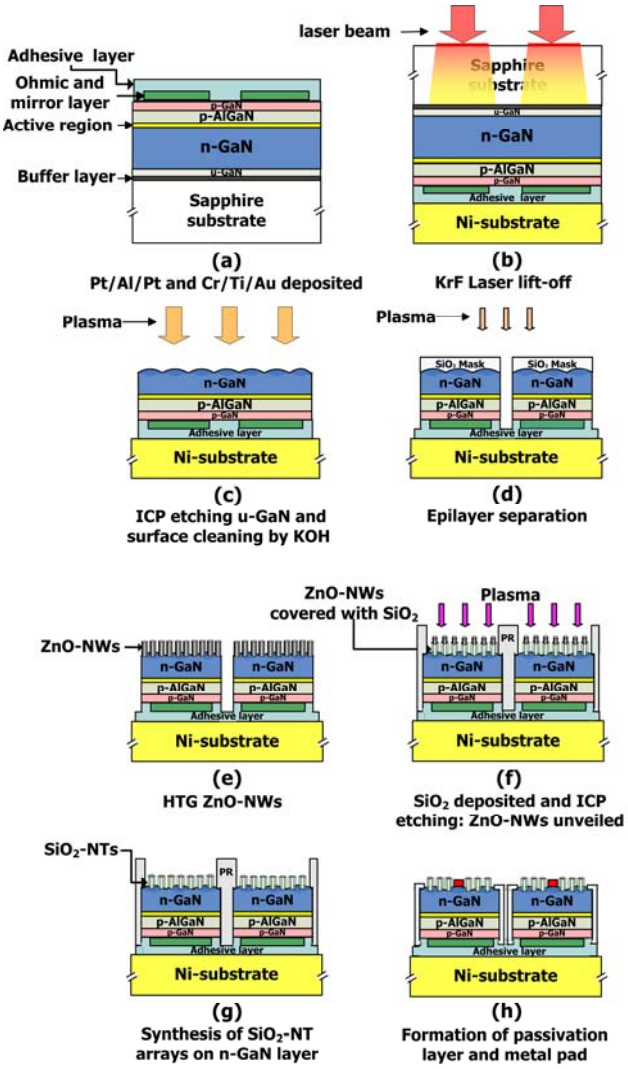

Fig. 1 Key fabrication processes of VLED with nano-roughened n-GaN top-surface by SiO_2-NT arrays.

3. Results and Discussion

A comparison of light transmittance among prepared samples grown on ITO-glass was shown in Fig. 2. One observes that SiO_2-NT arrays have a superior transmittance of around 92% in the visible light spectrum, which is higher than those of with ZnO-NW arrays only and with SiO_2–coated ZnO-NW arrays of the same geometry by about 12% and 14%, respectively.

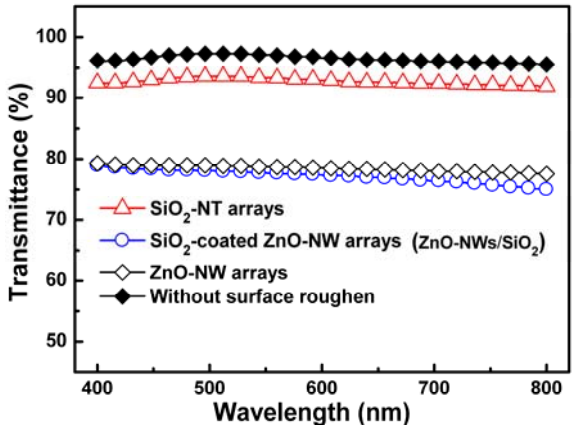

Fig. 2 The transmittance of prepared samples grown on ITO-glass substrate.

Figure 3 shows top surface morphologies of the prepared samples from scanning electron microscopy (SEM) at various processing stages. As shown in Fig. 3(a), it is seen that the hexagonal ZnO-NW arrays with an average length of 2 μm grown by HTG method were well-ordered and vertically-aligned. Figure 3(b) shows the surface morphology of ZnO-NWs fully coated with PECVD SiO_2 film, and Figure 3(c) shows that the top portion of SiO_2 layer was removed to expose the ZnO-NW tips right after the ICP process. Figure 3(d) shows the images of the prepared SiO_2-NTs with typical length of 1.5 μm and the top view exhibited in the inset. Note that SiO_2-NTs with controllable dimensions could be easily prepared via suitable control of process parameters for the growth of ZnO-NWs using HTG method and the deposition of a SiO_2 layer by a PECVD process.

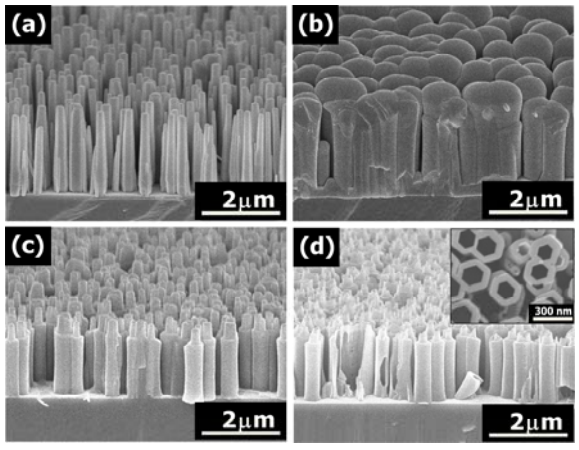

Fig. 3 SEM images of samples at various processing stages: (a) Growth of ZnO-NW arrays, (b) after the deposition of a SiO_2 film, (c) side-view of the sample after ICP etching, and (d) the side-view and top-view of SiO_2-NTs formed after the removal of ZnO-NWs.

The comparison of I-V and Lop-I characteristics of the fabricated various VLEDs with different surface texturing designs were shown in Fig. 4. No obvious difference was observed form their I-V characteristics, which indicates the proposed technology did not degrade the device electrical performance. At the same time, it also evident that the SiO_2-NT VLED has an additional improvement in Lop of about 49.8% at 350 mA and 40.6% at 750 mA as compared to regular VLED. Moreover, even as compared with ZnO-NW VLED and ZnO-NW/SiO_2 VLED, the SiO_2-NT VLED still achieved about 12.3% and 18% increments in Lop at 350 mA. Lop enhancement through the use of SiO_2-NT arrays can be attribute to the improved transmittance and to the boosted angular randomization of photons at the emission surface.

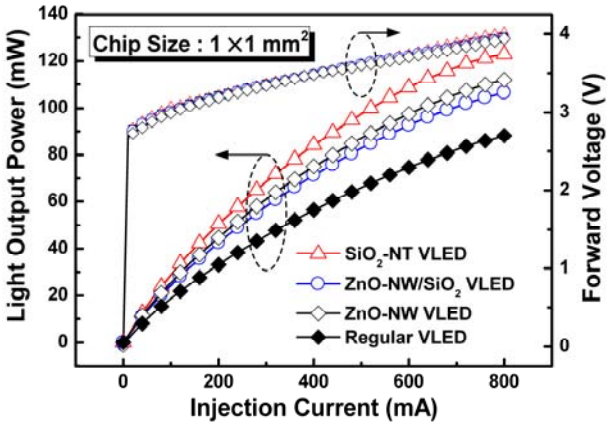

Fig. 4 Comparisons of I-V and L-I characteristics between various fabricated VLEDs.

4. Conclusion

In conclusion, surface texturing atop the n-GaN layer of high-power VLEDs using SiO_2-NT arrays were presented. Enhancement in Lop by 49.8%, 12.3%, and 18% at 350 mA as compared to regular, ZnO-NWs, ZnO-NWs/SiO_2 VLEDs, respectively, has been achieved. It is expected that the proposed SiO_2-NT arrays technology through the use of HTG ZnO-NWs as templates could be a potential surface roughening technique to further enhance the Lop of high power GaN-based LEDs for SSL in the near future.

Acknowledgments

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