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Degradation Mechanism for CLC Poly-Si n-TFTs under Low Vertical-Field HC Stress with Different Laser Annealing Powers

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1. Introduction

The continuous-wave green laser-crystallized (CLC) poly-silicon thin-film transistors (TFTs) [1] had been reported with its excellent output characteristic and high mobility. However, the TFTs exhibit different electrical characteristics under the identical process because of the grain boundary traps, grain traps and some defects on the channel region. All the traps and defects affect the characteristics of TFTs, especially in voltage stress. When the drain current of TFTs was increased, the large drain current possibly caused a serious reliability problem such as hot carrier effect (HCE) [2]. In this study, we observed and analyzed the variation of TFT characteristics under different laser annealing powers and different voltage stresses, especially on threshold voltage (V_T) and transconductance (G_M). The CLC poly-Si n-TFT device behavior is similar to a silicon-on-insulator (SOI) device operation. The bulk electrode is floating so that the impact ionization can not be clearly observed by bulk current. Hence, the capacitance deviations with frequencies were highly recommended to identify the interface states and bulk traps before and after stress.

2. Experimental

The CLC poly-Si n-TFT device was applied by a continuous-wave green laser crystallization to produce an epi-like silicon channel. Additionally, the gate dielectric TEOS-SiO_2 was deposited with 100-nm thickness by plasma-enhanced chemical vapor deposition (PECVD) technology at 300°C. Poly-Si gates and source/drain regions were doped with PH_3 ($5.0x10^{15}cm^{-2}$ and 35 keV), and activated by the thermal-furnace method for n-type TFTs. On the other hand, the active region of a TFT device was manufactured in channel poly-Si. The tested CLC poly-Si n-TFT was 15 um at width and 15 um at length. A cross-section view is shown in Fig. 1. Figures 2 (a) and (b) depict the microstructure of the poly-Si films crystallized by the CW green laser powers of 3.8W and 4.4W, respectively. The grain size of CLC device dealt with a lower CW green laser power was smaller than a higher one. Figure 3 displays the logarithmic transfer characteristics and linear transcondcutance curves with different laser annealing powers. From the experimental results, the TFTs were fabricated on poly-Si and crystallized by high CW green laser energy revealing excellent electrical characteristic and high electron mobility.

3. Results and Discussion

In this work, the used laser annealing powers were 3.75W and 4.25W. The output electrical characteristics with different annealing powers were exhibited in Fig. 4. When the device was crystallized by a larger energy power, the driving current was enhanced, and the transconductance was improved, too. Therefore, the reliability issue must be probed. For the stress conditions, the drain voltages were forced by 16, 18 and 20V, and the gate voltage was based on the threshold voltage for each device [3]. The stress time was from 0 to 3000 seconds under room temperature. While the carriers flow from source to drain terminal, the carriers are accelerated by a high lateral electric field and impact the lattice at the drain side to generate electron-hole pairs (EHPs). Therefore, the TFTs' local drain area and channel surface are usually damaged, which can be observed from the electrical characteristic curves. Figures 5 and 6 demonstrate the initial and stressed C_{GD}-V_G curves under two different laser annealing powers, respectively. For the decrease of C_{GD}, especially at high frequency, it is because that on the way to the drain terminal, the free electrons were easily caught by the trapped states coming from grain boundary. As the stress voltage increased, the degradation in V_T and G_M became serious. Figures 7 and 8 expose the ΔV_T and ΔG_M of low and high annealing energy powers. A schematic diagram of HCE stress for CLC TFT devices is shown in Fig. 9. Comparing Fig. 7 with Fig. 8, the G_M degradation is more serious. Typically, the G_M degradation is dependence of trapped states. Hence, the high laser annealing power caused more number of trapped states than that at low one.

4. Conclusions

The CLC poly-Si n-TFT with various laser annealing powers was investigated in this research. The degradation mechanism of device under voltage stress is dominated by HCE at the low vertical field. The hot carriers damage the drain side and the gate dielectric near the drain region. Therefore, the local defects were created which could be observed from sweeping C_{GD}-V_G curves. The critical factor is the location of interface traps and grain boundary trapped states. These traps are mainly attributed to the interface traps between SiO_2 and channel poly-Si, the grain boundary traps and the grain traps.

References

[1] Y.T. Lin *et al., APL*, **90** (2007) 073508.
[2] Satoshi Inoue *et al., JJAP*, **42** (2003) pp. 1168-1172.
[3] Yukiharu Uraoka *et al., JJAP*, **40** (2001) pp. 2833-2836.

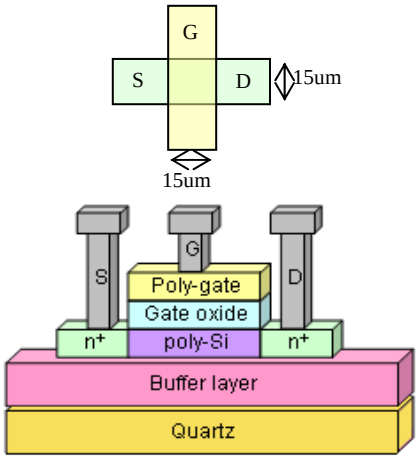

Fig. 1 An active area and cross-section diagram of the CLC poly-Si n-TFT.

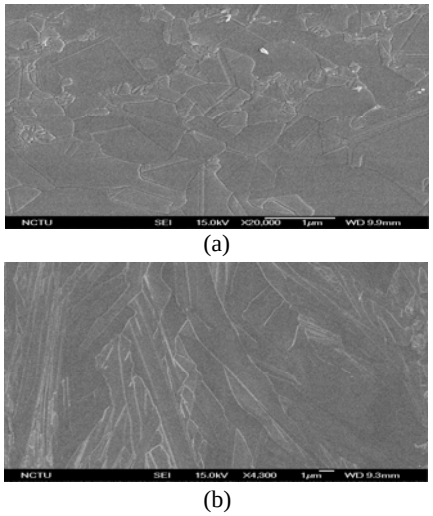

Fig. 2 SEM graph of the CLC poly-Si thin film crystallized at (a) 3.8W and (b) 4.4W.

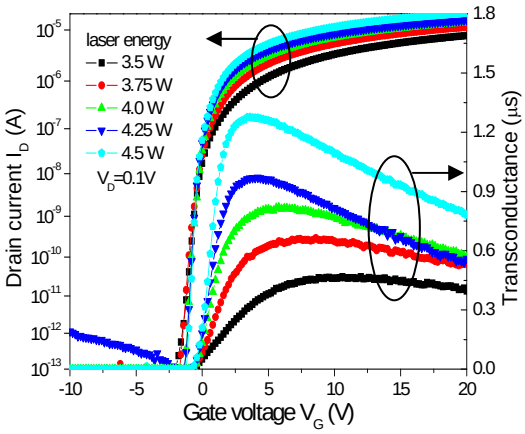

Fig. 3 I_D-V_G and G_M-V_G characteristic curves of the CLC poly-Si TFTs with different annealing powers.

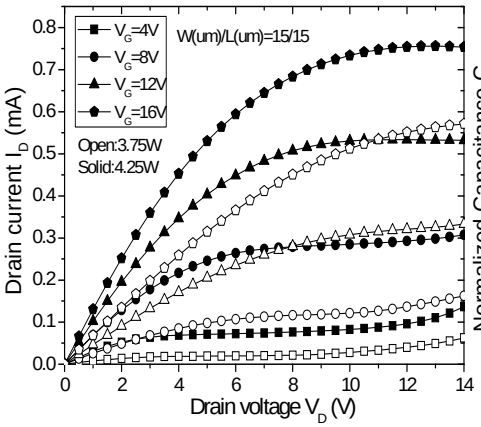

Fig. 4 Output characteristic curves of the CLC poly-Si TFTs with different annealing powers.

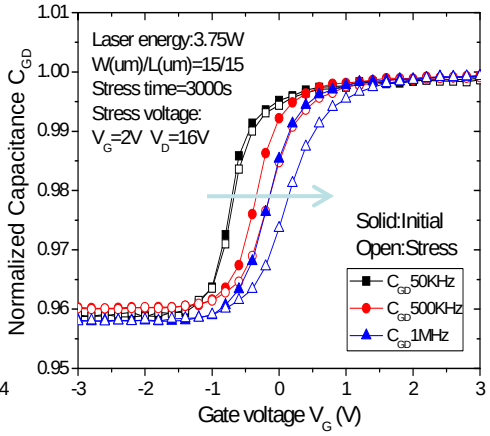

Fig. 5 C_{GD}-V_G curves of CLC poly-Si TFTs under HC effects at 3.75W.

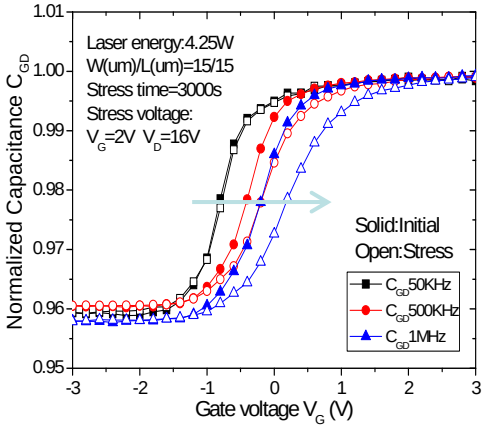

Fig. 6 C_{GD}-V_G curves of CLC poly-Si TFTs under HC effects at 4.25W.

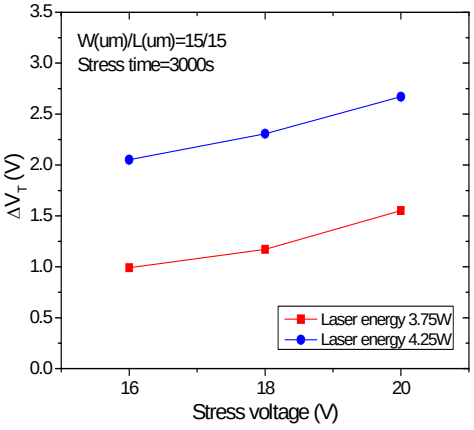

Fig. 7 Threshold voltage for CLC poly-Si TFTs under HC effects with different annealing powers.

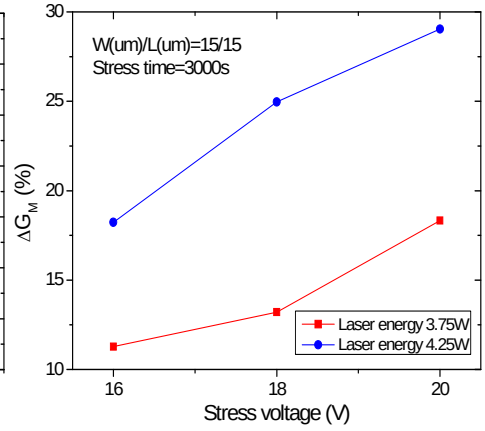

Fig. 8 Degradation of G_M for CLC poly-Si TFTs under HC effects with different annealing powers.

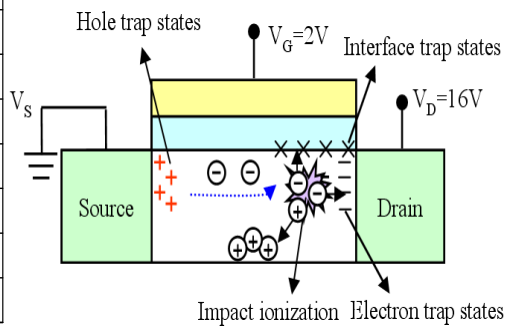

Fig. 9 Degradation mechanism of channel surface under HC effects for CLC poly-Si TFT.