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Electric properties of SONOS memories with embedded silicon nanocrystals in nitride

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Abstract

This study investigates the electrical properties of SONOS memories with embedded silicon nanocrystals (Si-NC) in nitride. The interface states at the SiO_2/Si-substrate interface are identified by experiment and simulation. Embedded Si-NCs in nitride are confirmed as a formation of Si-quantum dots in nitride. The Si-NCs form quantum confined states above their conduction band (CB). The electron capture time of the Si-quantum dots states is increased during programming carriers. This mechanism reveals that the Si-quantum dots states are effortless to program, and that the electrons on these states after programming can be reserved more easily.

Introduction

Metal–oxide–semiconductor (MOS) memories with embedded Si-NCs and silicon–oxide–nitride–oxide–silicon (SONOS) nonvolatile memories have recently attracted considerable attention because of their feasibility to overcome the limitations of conventional polycrystalline-silicon-based floating-gate memories [1]-[3]. Our previous works successfully demonstrated SONOS memories with embedded Si-NCs in silicon nitride [4]-[5]. This novel structure exhibits excellent characteristics in terms of larger memory windows, lower operation voltage, high P/E speed, and longer retention time. Nevertheless, the fundamental electric properties of this structure remain unknown.

Experiments

Figure 1 presents the device structure of the investigated samples. The SONOS memories with embedded Si-NCs are formed by *ex situ* deposition in nitride. Detailed growth conditions can be found elsewhere [4]-[5]. A series of various Si-NC size (no Si-NC (no_dot), small Si-NCs (small_dot), and large Si-NCs (dot)) are investigated in this work. The formation of Si-NCs was confirmed by atomic force microscopy [4].

Results and Discussion

Figure 2 shows the capacitance-voltage (C-V) spectra (dashed line) of, and the corresponding simulation results (solid line) for, the investigated samples ((a) no_dot, (b) small_dot, and (c) dot). All of these samples have an additional capacitance peak in the positive bias region. The additional capacitance peak originates from the interface states at the SiO_2/Si-substrate interface. The fundamental parameters (Dit (interface state density) and N_{Qss} (fixed oxide charges)) can be extracted by C-V simulation. The energy distributions of interface state density in the silicon band gap are extracted from C-V simulation, as shown in Fig. 3. These energy distributions are consistent with the previous non-annealing results [6]. The N_{Qss} are increased during the formation of Si-NCs. This result suggests that the embedded Si-NCs increase the number of trapping states in the oxide region, and trapping states are increased through enlarging the Si-NC size. Admittance spectroscopy was performed on these samples to investigate the emission time of the interface states. Figure 4 shows the temperature-dependent capacitance-frequency (C-F) spectra at bias of the additional capacitance maximum peak ((a) 2 V for no_dot, (b) 1.8 V for small_dot, and (c) 1.4 V for dot), and other biases of the additional capacitance peak exhibit the same temperature-dependent behavior. The dependence of the inflection frequency on temperature yields an activation energy (Ea) and a capture cross section (σ), as indicated in Table 1 (Ea, σ, and Ea from simulation). The similarity between the experimental activation energy and the simulated value at small bias confirms that the additional capacitance peak originates from the interface states at the SiO_2/Si-substrate interface. The discrepancy at large bias is caused by the phonon-assisted tunneling in a large electric field [7], as shown in Fig. 5.

Deep-level transient spectroscopy (DLTS) is applied in further investigation of the trapping states in the oxide region. Figure 6 shows the bias-dependent DLTS spectra of the investigated samples ((a) no_dot, (b) small_dot, and (c) dot). All of these samples have an apparent peak (E_i). The dot-sample has an additional peak (E_d) as the bias is swept from 2 to 3 V, as shown in Fig. 6 (c) (indicated by an arrow). According to the bias, emission time, and activation energy, the electric state of the apparent peak (E_i) originates from the interface state, which was analyzed above. Thus, the additional peak (E_d) of the dot-sample originates from the trapping states in the oxide region. Since these trapping states are not observed in the no_dot-sample, they are related to Si-NCs. These trapping states are examined in detail by simulating the band structure. Table 2 shows the activation energy (Ea) and capture cross section (σ) that were obtained from these trapping states by DLTS; the band structure simulation is based on the biases that were applied in this experiment. Figure 7 shows the simulated band structure for (a) V_G= -2.24 V (flat-band voltage) and (b) V_G= 1.8 V. This simulated band structure reveals that the Fermi level is close to Si-NCs when the trapping states are measured. This result demonstrates that the signal of the trapping states is produced by the Si-NCs. The simulation of the band structure reveals other important mechanisms. At applied biases of 2 V to 3.5 V, the Fermi level is swept through the CB of Si-NCs. This consequence reveals that the Si-NCs form quantum confined states above the CB of Si-NCs, and the trapping states below the CB of Si-NCs are probably the localized states that are produced by the composition fluctuation of Si-NCs. The above results demonstrate that embedded Si-NCs in nitride act as a formation of Si-quantum dots in nitride.

Programming carriers is applied to understand the variation of electric properties after "WRITE" operation. Figure 8 shows the DLTS spectra of the dot-sample under three conditions ((a) no-programmed, (b) less-programmed, and (c) programmed). Excluding the voltage shift, the properties (activation energy and capture cross section) of the SiO_2/Si-substrate interface states remain almost unchanged, as indicated in Table 3. Therefore, the time constant of the interface states at the SiO_2/Si-substrate is fixed to observe the time constant of the Si-quantum dots states. The time constant of the Si-quantum dots states increases during programming carriers, as shown in Fig. 8 (indicated by an arrow), leading to the increase of the activation energy, as indicated in Table 4. Based on DLTS theory [8], the peak of the Si-quantum dots states originates from the hole emission or the electron capture. According to the simulation of the band structure, the peak of the Si-quantum dots states originates from the electron capture, and the time constant corresponds to the capture time of these states. The increase of the activation energy during programming carriers suggests that the electrons cannot easily be transported into Si-quantum dots states after programming carriers, and that the electrons on Si-quantum dots states also cannot easily be transported into the Si-substrate CB. Based on this mechanism, the Si-quantum dots states can be effortlessly programmed (~330 meV), and the electrons on these states after programming can be reserved more easily (~430 meV).

Conclusions

This study elucidates the fundamental electric properties of SONOS memories with embedded Si-NCs in nitride. Initially, the interface states at the SiO_2/Si-substrate are identified by experiment and simulation. Embedded Si-NCs in nitride are confirmed as a formation of Si-quantum dots in nitride. The electron capture time of the Si-quantum dots states is increased during programming carriers. This mechanism suggests that the electrons on these states can be reserved more easily after programming.

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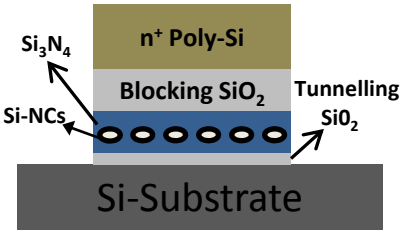

Fig. 1 The device structure of investigated samples.

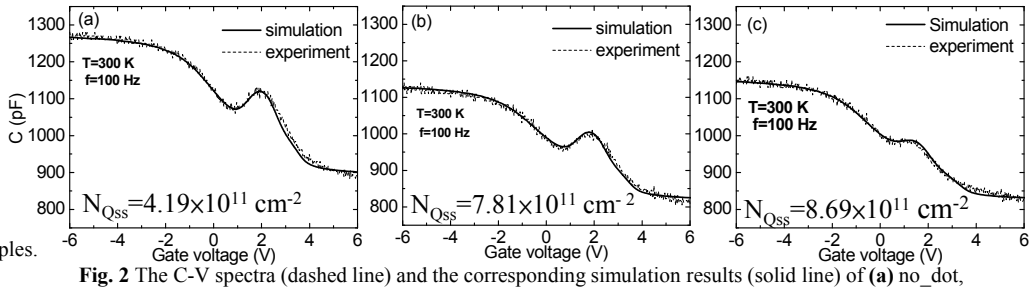

Fig. 2 The C-V spectra (dashed line) and the corresponding simulation results (solid line) of **(a)** no_dot, **(b)** small_dot, and **(c)** dot sample.

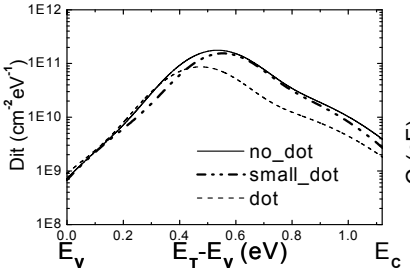

Fig. 3 The energy distributions of interface state density in silicon band gap.

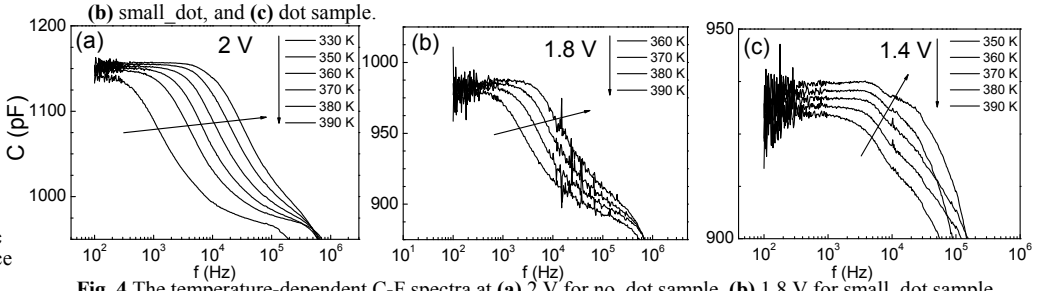

Fig. 4 The temperature-dependent C-F spectra at **(a)** 2 V for no_dot sample, **(b)** 1.8 V for small_dot sample, and **(c)** 1.4 V for dot sample).

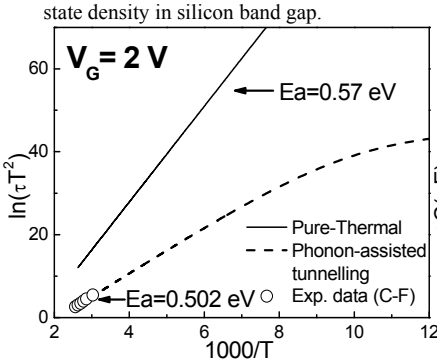

Fig. 5 The simulation of phonon-assisted tunneling for no_dot sample under large electric field.

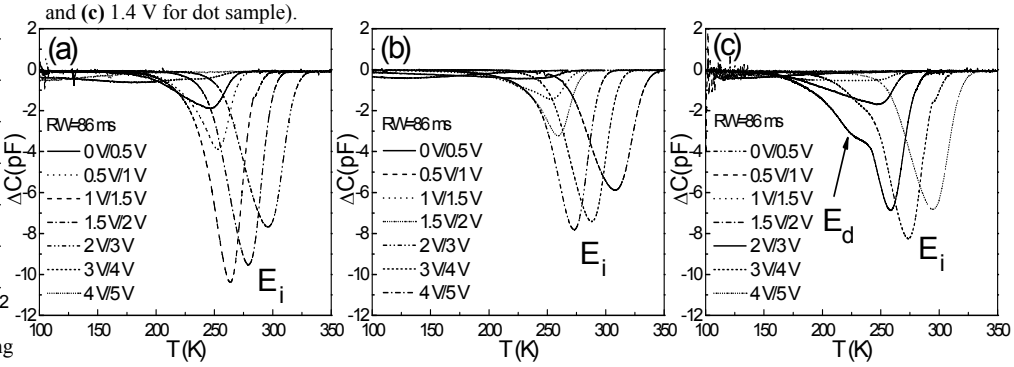

Fig. 6 The bias-dependent DLTS spectra of **(a)** no_dot, **(b)** small_dot, and **(c)** dot sample.

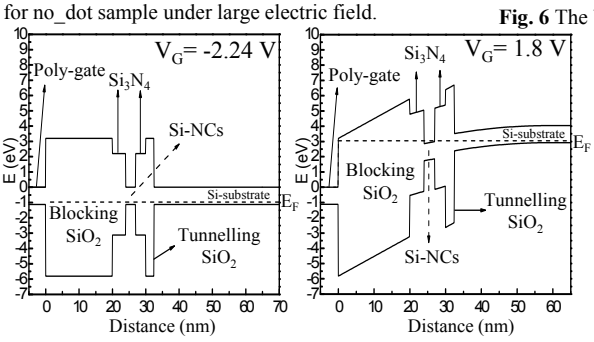

Fig. 7 The bandstructure simulation of **(a)** V_G=-2.24 V (flat-band voltage) and **(b)** V_G=1.8 V.

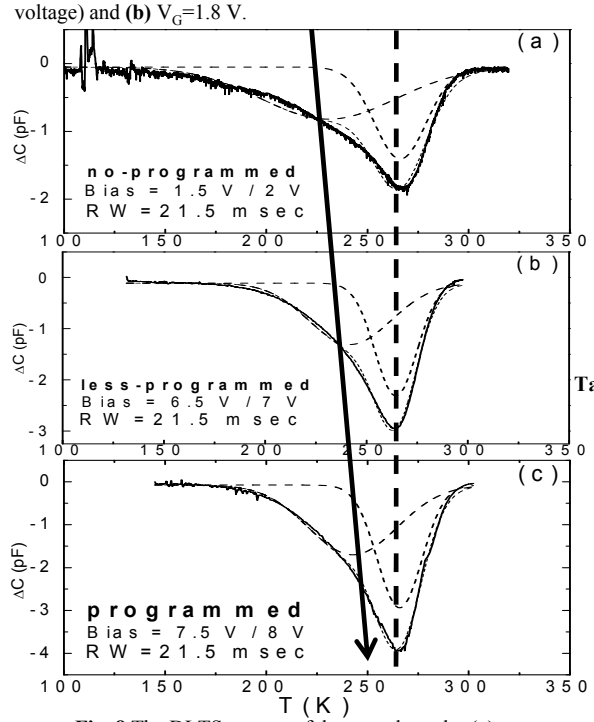

Fig. 8 The DLTS spectra of dot-sample under **(a)** no-programmed, (b) less-programmed, and **(c)** programmed.

SiO_2/Si-substrate interface peak											
no_dot sample				small_dot sample				dot sample			
Bias(V)	Ea(eV)	σ (cm^2)	Ea(eV) sim.	Bias(V)	Ea(eV)	σ (cm^2)	Ea(eV) sim.	Bias(V)	Ea(eV)	σ (cm^2)	Ea(eV) sim.
1.2	0.457	6.5×10^{-17}	0.399	1.2	0.47	8.1×10^{-17}	0.45	1.2	0.503	5.58×10^{-16}	0.479
1.4	0.476	8.7×10^{-17}	0.439	1.4	0.519	6.74×10^{-16}	0.489	1.4	0.469	1.3×10^{-16}	0.52
1.6	0.493	1.23×10^{-16}	0.48	1.6	0.57	3.2×10^{-15}	0.529	1.6	0.512	4.7×10^{-16}	0.562
1.8	0.497	1.19×10^{-16}	0.524	1.8	0.588	4.88×10^{-15}	0.571	1.8	0.539	4.51×10^{-16}	0.605
2	0.502	1.2×10^{-16}	0.57	2	0.597	6.08×10^{-15}	0.614	2	0.534	3.2×10^{-16}	0.65
2.2	0.505	1.14×10^{-16}	0.617	2.2	0.638	2.23×10^{-14}	0.659	2.2	0.536	2.77×10^{-16}	0.697
2.4	0.508	1.09×10^{-16}	0.666	2.4	0.602	6.02×10^{-14}	0.705	2.4	0.537	2.42×10^{-16}	0.745
2.6	0.506	8.7×10^{-17}	0.717	2.6	0.596	4.46×10^{-15}	0.752	2.6	0.54	2.27×10^{-16}	0.794
2.8	0.518	1.11×10^{-16}	0.769	2.8	0.609	5.84×10^{-15}	0.801	2.8	0.543	2.14×10^{-16}	0.845
3	0.51	7.1×10^{-17}	0.823	3	0.604	4.24×10^{-15}	0.852	3	0.543	1.81×10^{-16}	0.897
3.2	0.52	8.1×10^{-17}	0.879	3.2	0.629	8.3×10^{-15}	0.903	3.2	0.547	1.71×10^{-16}	0.95
3.4	0.519	6.4×10^{-17}	0.935	3.4	0.588	1.93×10^{-15}	0.955	3.4	0.587	4.93×10^{-16}	1.001

Table 1 Comparisons of Ea from C-F measurement, σ from C-F measurement, Ea from simulation.

Si-NCs related peak		
Bias(V)	Ea(eV)	σ (cm^2)
1.5V / 2V	0.338	1.26×10^{-17}
2V / 2.5V	0.334	2.31×10^{-18}
2.5V / 3V	0.319	7.91×10^{-19}
3V /3.5V	0.337	7.84×10^{-19}

Table 2 Comparisons of Ea and σ from DLTS measurement.

Si-NCs related peak					
no-programmed			less-programmed		
Bias(V)	Ea(eV)	σ (cm^2)	Bias(V)	Ea(eV)	σ (cm^2)
1.5V / 2V	0.338	1.26×10^{-17}	6V / 6.5V	0.370	2.09×10^{-17}
2V / 2.5V	0.334	2.31×10^{-18}	6.5V / 7V	0.363	6.88×10^{-18}
2.5V / 3V	0.319	7.91×10^{-19}	programmed		
3V /3.5V	0.337	7.84×10^{-19}	Bias(V)	Ea(eV)	σ (cm^2)
			7V / 7.5V	0.437	5.76×10^{-16}
			7.5V / 8V	0.438	5.53×10^{-16}

Table 4 Comparisons of Ea and σ under different programming conditions.

SiO_2/Si-substrate interface peak		
no-programmed		
Bias(V)	Ea(eV)	σ (cm^2)
2	0.472	7.98×10^{-17}
2.5	0.472	5.09×10^{-17}
3	0.473	3.52×10^{-17}
3.5	0.484	3.41×10^{-17}
4	0.499	3.51×10^{-17}
4.5	0.532	5.55×10^{-17}
5	0.559	7.04×10^{-17}
programmed		
Bias(V)	Ea(eV)	σ (cm^2)
3.4	0.458	9.05×10^{-17}
3.9	0.490	1.49×10^{-16}
4.4	0.480	7.39×10^{-17}
4.9	0.489	6.22×10^{-17}
5.4	0.499	5.36×10^{-17}
5.9	0.518	5.66×10^{-17}
6.4	0.543	6.37×10^{-17}

Table 3 Comparisons of Ea and σ under different programming conditions.