Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp473-474

# Source Engineering for Tunnel Field-Effect Transistor: Elevated Source with Vertical Silicon-Germanium/Germanium Heterostructure

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## 1. Introduction

The Tunneling field-effect transistor (TFET) is a promising candidate for ultra-low power applications due to its superior off-state and subthreshold characteristics and its potential to work at supply voltages well below 0.5 V [1] - [3]. $Si_{1-z}Ge_z$/Si and Ge/Si structures are attractive for boosting the performance of Si-based TFETs. A Si TFET structure with an inserted $Si_{1-z}Ge_z$ layer between the $p^+$ Si source and channel was recently reported [4], [5].

In this work, we fabricated Si-based TFETs with a vertical $Si_{0.5}Ge_{0.5}$ source and investigated the impact of inserting an undoped Ge layer in the source for performance enhancement (Fig. 1). The Ge layer suppresses diffusion of boron (B) into the Si channel, and reduces the tunnel barrier for a given bias. Compared with a control device without the Ge layer, TFETs with a $Si_{0.5}Ge_{0.5}$/Ge source show a higher $I_{ON}$, improved threshold voltage ($V_{TH}$) and subthreshold characteristics.

## 2. Device Design and Simulation

Fig. 1(a) shows the schematic of a TFET with an undoped Ge layer inserted between B-doped $Si_{0.5}Ge_{0.5}$ and Si channel (denoted as $Si_{0.5}Ge_{0.5}$/Ge source) for suppressing B diffusion into Si and reducing the tunnel barrier. Fig. 2 shows simulated $I_{DS}$-$V_{GS}$ curves of TFETs with $Si_{0.5}Ge_{0.5}$ source [Fig. 1(b)] with different source doping profiles. A more gradual B profile increases $V_{TH}$ and degrades subthreshold swing (*SS*).

Fig. 3 shows the energy band diagram, active B and hole profiles along source-to-channel direction in TFETs, where the $Si_{0.5}Ge_{0.5}$ is B-doped at $8\times10^{20}$ $cm^{-3}$ and decays at 2 nm/decade towards the channel. The Ge layer helps to increase the local electric field and effectively reduces the tunnel barrier. Consequently, the TFET with $Si_{0.5}Ge_{0.5}$/Ge source has a higher generation rate (Fig. 4). Details of the simulation method employed were described elsewhere [6].

## 3. Device Fabrication

TFETs studied in this work were fabricated on 6" *p*-type (100) Si wafers (4-8 Ω·cm). Key process steps are illustrated in Fig. 5.

Drain regions were formed by masked $As^+$ implants at 50 keV and a dose of $10^{15}$ $cm^{-2}$, followed by rapid thermal annealing (RTA) at 1000 ºC for 10 s for dopant activation. B-doped $Si_{0.5}Ge_{0.5}$ on undoped Ge was grown at 480 ºC to form the source. Hall measurement indicates that the active B concentration in $Si_{0.5}Ge_{0.5}$ is $8\times10^{20}$ $cm^{-3}$. A $SF_6$-based etch step removed the $Si_{0.5}Ge_{0.5}$/Ge in the drain region and formed the elevated $Si_{0.5}Ge/_{0.5}Ge$ source region. The gate stack comprises a 100 nm TaN on 5 nm $Al_2O_3$ formed by atomic layer deposition (ALD). For control device, a single B-doped $Si_{0.5}Ge_{0.5}$ layer was used as the source. Fig. 6 shows the TEM images of a TFET with $Si_{0.5}Ge_{0.5}$/Ge source.

## 4. Results and Discussion

Fig. 7 shows the SIMS profiles for B and Ge along the vertical direction in source region of TFETs with and without the Ge layer. As the diffusivity of boron in Ge is much lower than that in Si, the inserted Ge layer suppresses boron diffusion into Si, and results in a steeper source doping profile.

Fig. 8 and 9 show the electrical characteristics of the TFET with $Si_{0.5}Ge_{0.5}$/Ge source. As compared with the control TFET, a higher $I_{ON}$ and enhanced SS characteristics (Fig. 10) are achieved.

The $I_{ON}$ enhancement could be attributed to the following reasons. Firstly, the Ge layer with smaller band gap reduces the tunnel barrier. Secondly, the valence band shift and splitting induced by compressive strain in Ge layer increase the valence band offset at Ge/Si interface, which reduces the tunnel barrier further. Thirdly, higher tensile strain is induced in the Si channel, leading to the increase of conduction band offset at the tunneling junction, which could also contribute to tunnel barrier reduction. Finally, the smaller tunneling mass in Ge layer could also contribute to the enhancement of the tunneling current. The improved $V_{TH}$ and *SS* are mainly attributed to the suppression of the diffusion B into the channel region.

## 5. Conclusion

Source engineering for TFET with *in situ* B-doped $Si_{0.5}Ge_{0.5}$ source was investigated. A Ge layer inserted beneath the $Si_{0.5}Ge_{0.5}$ source effectively increased the $I_{ON}$ and subthreshold swing of the TFET due to the reduction of tunnel barrier and the suppression of B diffusion into Si channel.

**Acknowledgement.** We acknowledge a research grant (NRF-RF2008-09) from National Research Foundation (NRF).

**References**

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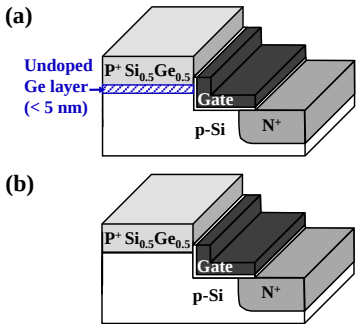


Fig. 1. Schematics of (a) a TFET with a vertical $Si_{0.5}Ge_{0.5}$/Ge source and (b) a TFET with $Si_{0.5}Ge_{0.5}$ source (control). In (a), a 5 nm undoped Ge layer was grown beneath the $Si_{0.5}Ge_{0.5}$ region.

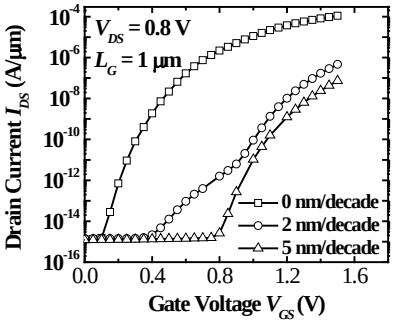


Fig. 2. Simulated $I_{DS}$-$V_{GS}$ curves of TFET with $Si_{0.5}Ge_{0.5}$ source and with different source doping profiles. Boron diffusion into the Si channel increases the threshold voltage and affects the subthreshold swing.

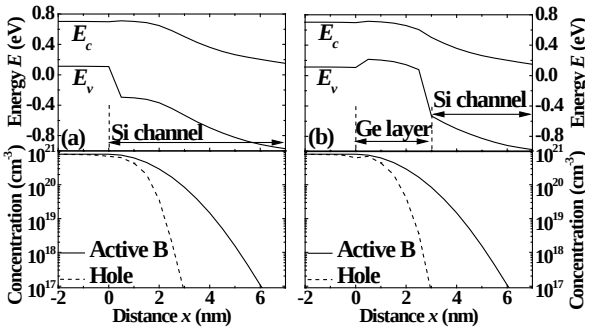


Fig. 3. Simulated energy band diagram (top), and active Boron and hole profiles (bottom) along source-to-channel direction in TFET (a) with $Si_{0.5}Ge_{0.5}$ source, and (b) $Si_{0.5}Ge_{0.5}$/Ge source. $V_{GS}$ = 0.1 V and $V_{DS}$ = 0.8 V. The gate edge is at $x$ = 0. The local electric field at the tunneling junction is higher in (b).

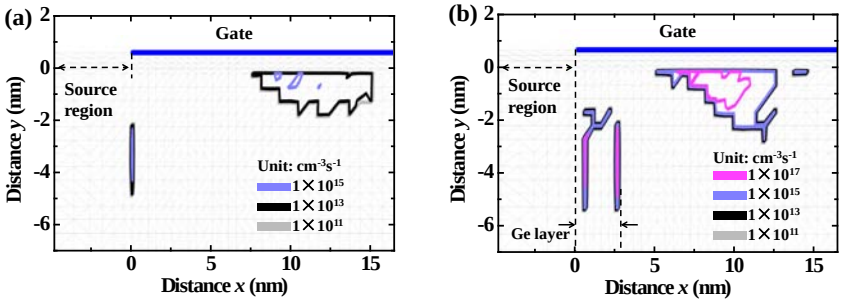


Fig. 4. Simulated electron and hole generation rate contours for TFETs (a) with $Si_{0.5}Ge_{0.5}$ source (control) and (b) with $Si_{0.5}Ge_{0.5}$/Ge source. $V_{GS}$ = 0.1 V and $V_{DS}$ = 0.8 V. The generation rate is higher and the tunneling barrier is reduced in the TFET with $Si_{0.5}Ge_{0.5}$/Ge source.

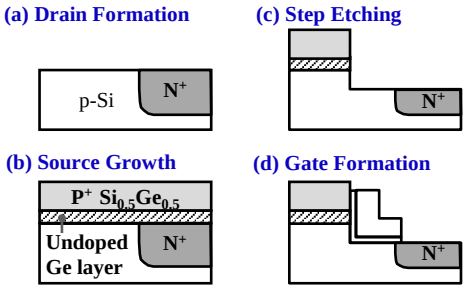


Fig. 5. Process flow used to fabricate TFET with $Si_{0.5}Ge_{0.5}$/Ge source. For the control TFET, $Si_{0.5}Ge_{0.5}$ source was grown.

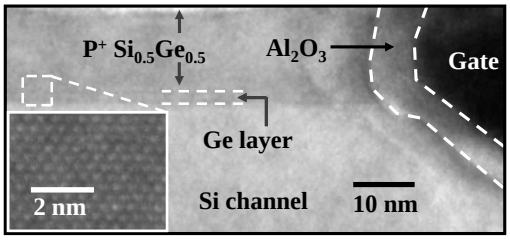


Fig. 6. TEM image of TFET featuring TaN metal gate, $Al_2O_3$ gate dielectric, and $Si_{0.5}Ge_{0.5}$/Ge source. The inset shows high-resolution TEM image revealing the excellent crystalline quality of the $Si_{0.5}Ge_{0.5}$/Ge source.

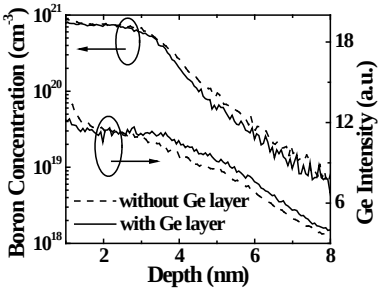


Fig. 7. SIMS profiles for B (left) and Ge (right) along the vertical direction in source of TFETs with and without Ge layer. The inserted Ge layer reduces B diffusion into Si channel.

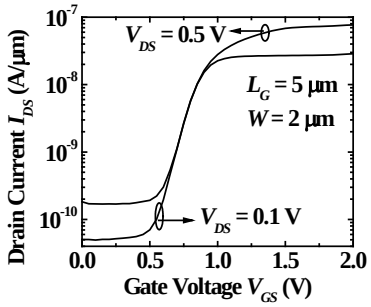


Fig. 8. Experimental $I_{DS}$-$V_{GS}$ curves of TFET with $Si_{0.5}Ge_{0.5}$/Ge source.

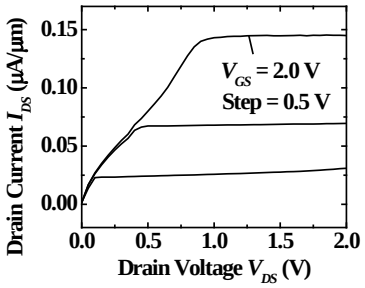


Fig. 9. Experimental $I_{DS}$-$V_{DS}$ curves of TFET with $Si_{0.5}Ge_{0.5}$/Ge source.

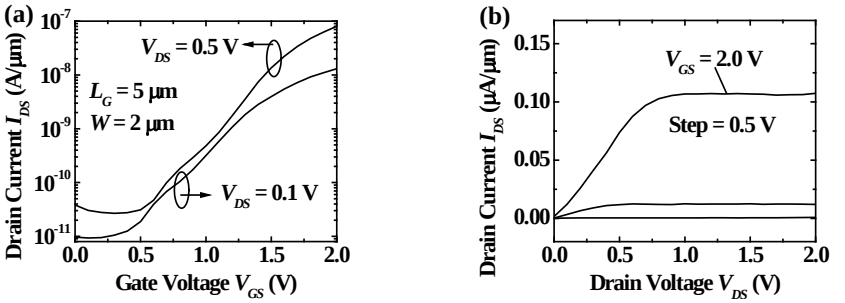


Fig. 10. Experimental (a) $I_{DS}$-$V_{GS}$ and (b) $I_{DS}$-$V_{DS}$ curves of control TFET. Compared to the TFET with $Si_{0.5}Ge_{0.5}$/Ge source, the control device shows a lower $I_{ON}$, worse $V_{TH}$ and subthreshold characteristics.