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High-Performance Polycrystalline Silicon Thin-Film Transistor with Nickel-Titanium Oxide by Sol-Gel Spin-Coating and Fluorine Implantation

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Abstract

A high-performance poly-Si TFTs is reported without additional hydrogenation or advanced phase crystallization techniques. Excellent electrical characteristics are attributed to the promising high-κ $NiTiO_3$ by sol-gel spin-coating and the trap passivation by fluorine implantation. Meanwhile, the hot-carrier reliability is greatly improved by the robust Si-F bonds.

Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention because of their various applications, such as driving circuits of the active matrix liquid crystal displays (AM-LCDs) and those of the active matrix organic light emitting diode displays (AM-OLEDs) [1] [2]. Nickel-titanium oxide ($NiTiO_3$) deposited by physical vapor deposition was shown to be a promising high dielectric constant (high-κ) gate dielectric [3]. Recently, we have reported a p-channel poly-Si TFT with the $NiTiO_3$ gate dielectric by sol-gel spin-coating [4]. To further improve the TFT characteristics, defect passivation such as hydrogen plasma treatment is often necessary. However, weak Si-H bonds tend to degrade device reliability. Fluorine implantation was reported to passivate defects by more robust Si-F bonds [5]. In this paper, high performance n-channel poly-Si TFTs is reported by taking advantage of the high-κ $NiTiO_3$ gate dielectric by sol-gel spin-coating and the fluorine implantation.

Device Fabrication and Experimental Procedures

The schematic of the poly-Si TFT with TaN metal gate and $NiTiO_3$ gate dielectric is shown in Fig. 1. First, 50-nm amorphous silicon (a-Si) was deposited on 550-nm SiO_2 by low-pressure chemical vapor deposition (LPCVD) at 550°C, followed by the fluorine implantation with projected ion range at the middle of a-Si film and dosage of $5 \times 10^{13} cm^{-2}$. The a-Si layer was subjected to recrystallization at 600°C for 24 h in N_2 ambient, and the photolithography patterning of the active region. The N^+ source and drain were done by phosphorus implantation and activation at 600°C for 12 h. Next, $NiTiO_3$ film was spin-coated on a 3-nm SiO_2 layer using a $NiTiO_3$ sol-gel solution and then baked at 200°C for 10 min to remove the solvent. The sol-gel solution was synthesized by dissolving nickel acetate tetrahydrate [$Ni(OOCCH_3)_2 \cdot 4H_2O$] and titanium isopropoxide [$Ti(O^iPr)_4$] in 2-methoxyethanol. The $NiTiO_3$ spin-coating process was repeated for 3 times to obtain a film thickness of about 50 nm. After thermal treatment at 400°C in O_2 ambient for 20 min, the samples were subjected to additional rapid thermal annealing (RTA) at 500°C for 30 s in N_2 ambient. The gate was defined by TaN deposition and lift-off process. Then, a 400 nm SiO_2 passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). To open the contact holes, SiO_2 and $NiTiO_3$ were etched by buffered oxide etch (BOE) and $HF:H_2O$ = 50:1, respectively. Finally, aluminum pads were defined. The poly-Si TFT with $NiTiO_3$ gate dielectric but without fluorine implantation was also fabricated using the same process flow for comparison.

Results and Discussion

As shown in Fig. 2, an accumulation capacitance density of 410 nF/cm^2 is achieved for the $NiTiO_3$ film from capacitance-voltage (C-V) measurement, corresponding to the equivalent-oxide thickness (EOT) of 8.4 nm and the effective dielectric constant value of 23.2. Figure 3 shows the transfer characteristics of the poly-Si TFTs with and without fluorine implantation at V_{DS} = 0.1 V and 1 V, respectively. The electrical characteristics of the fluorine-implanted TFT were significantly improved compared to the one without. The threshold voltage (V_{TH}) and the subthreshold swing were decreased from 1.49 to 1.09 V and from 262 to 207 mV/dec., respectively. In addition, the field-effect mobility was increased from 47.5 to 56.7 cm^2/V-s. The output characteristics of the TFTs with and without the fluorine implantation are shown in Fig. 4. The driving current of the fluorine-implanted TFT had about 60 % improvement at V_{GS}-V_{TH} = 4 V, compared to that without fluorine implantation. The improvements of the electrical performance could be attributed to the passivation of interface states at the gate dielectric/poly-Si interface and trap states in the poly-Si film by the incorporation of fluorine [5].

In order to verify the effect of fluorine passivation, the effective trap-state density (N_{trap}) at grain boundaries was calculated from the grain-boundary trapping model proposed by Levinson *et al.* [6]. Figure 5 depicts the $\ln[(I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ at V_{DS} = 0.1 V. The extracted N_{trap} were 3.8×10^{12} cm^{-2} and 6.6×10^{12} cm^{-2} for the TFTs with and without fluorine implantation, respectively. This result indicated that the incorporation of fluorine can effectively passivate the trap states at grain boundaries.

Additionally, hot-carrier stress was carried out by V_{DS} = V_{GS} = 4V to investigate the instability of TFTs. The V_{TH} shift due to the broken Si-Si and Si-H bonds at the gate dielectric/ poly-Si interface during hot-carrier stress is shown in Fig. 6. The TFT with fluorine implantation has better immunity against the hot-carrier stress owing to stronger Si–F bond compared with weaker Si–H and Si–Si bonds in the poly-Si channel region. Finally, the key parameters were summarized in Table I.

Conclusion

High-performance poly-Si TFTs with high-κ $NiTiO_3$ gate dielectric by sol-gel spin-coating and fluorine implantation have been demonstrated. The superior dielectric properties of high-κ $NiTiO_3$ lead to high gate capacitance density. Both the DC electrical characteristics and hot-carrier reliability are significantly improved by the fluorine implantation and $NiTiO_3$ gate dielectric, suggesting its promise for high-speed and low-power display driving circuits.

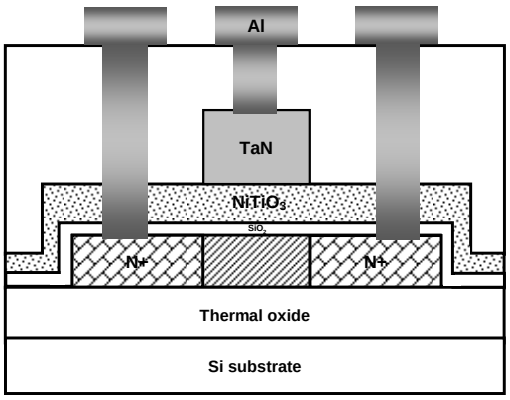

Fig. 1. The schematic of the poly-Si TFT with $NiTiO_3$ gate dielectric.

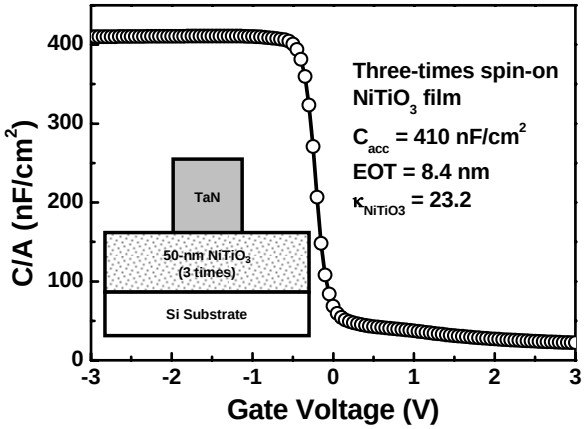

Fig. 2. C-V curve of the high-κ $NiTiO_3$ capacitor.

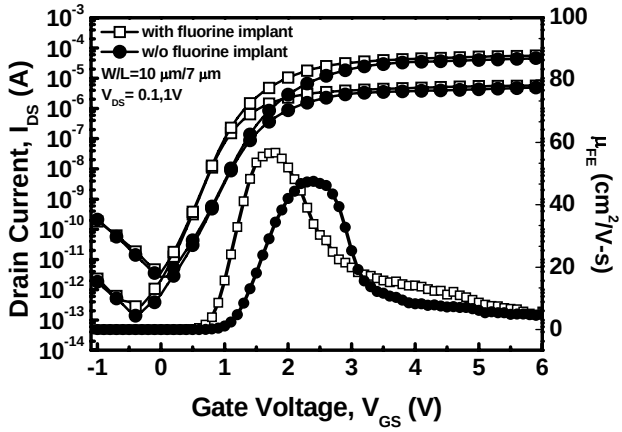

Fig. 3. Transfer characteristics of poly-Si TFTs with and without fluorine implantation.

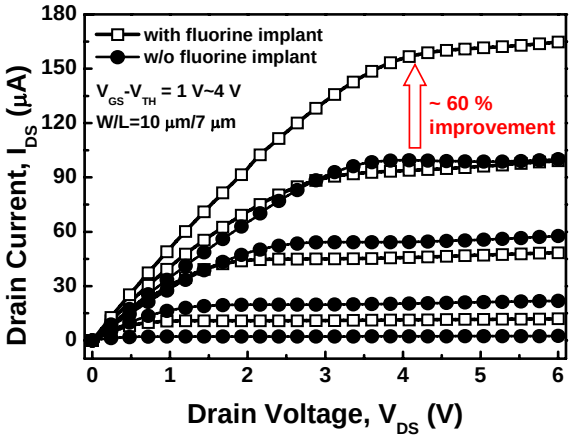

Fig. 4. Output characteristics of poly-Si TFTs with and without fluorine implantation.

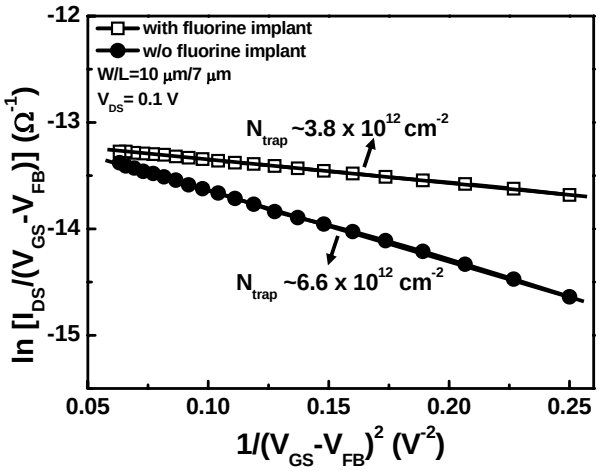

Fig. 5. Effective trap-state densities of poly-Si TFTs with and without fluorine implantation..

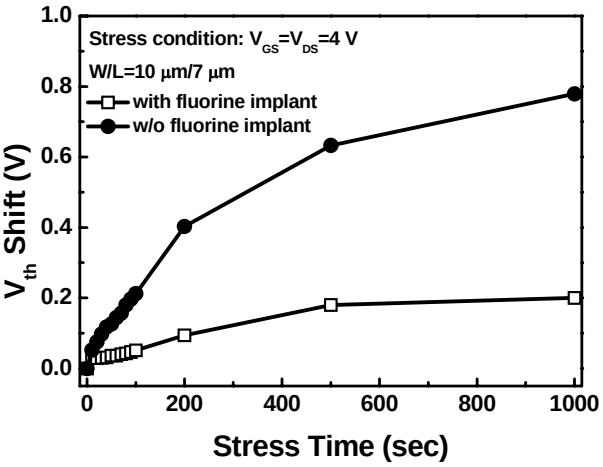

Fig. 6. Threshold voltage shift versus stress time for poly-Si TFTs with and without fluorine implantation.

Table I. Summary of electrical characteristics for poly-Si TFTs with and without fluorine implantation.

Poly-Si $NiTiO_3$ TFT	V_{TH} (V)	S.S. (mV/dec.)	μ_{FE} (cm^2/V-s)	I_{ON}/I_{OFF} Ratio	N_{trap} (cm^{-2})	ΔV_{TH} (V)
With Fluorine	1.09	207	56.7	$1.48x10^7$	$3.8x10^{12}$	0.2
W/O Fluorine	1.49	262	47.5	$1.7x10^7$	$6.6x10^{12}$	0.78

References

[1] Y. Chen, et al., IEDM Tech. Dig. 389, (2002).
[2] J. Engel, et al., Proc. Mat. Res. Soc. Symp.736, D.4.5.1, (2003).
[3] T. M. Pan, et al., Appl. Phys. Lett. 78, 1439, (2001)
[4] S. C. Wu , et al., int. Conf. on SSDM., 583, (2009)
[5] C. K. Yang, et al., J. Electrochem. Soc. 143, 3302 (1996)
[6] J. Levinson et al., J. Appl. Phys. 53, 1193 (1982).