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More Moore and More than Moore Meeting for 3D in the 21st Century

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1. Introduction

Nanoelectronics linear scaling appeals new 3D integration schemes in order to continue Moore's law. Unique opportunities exist to increase the devices performances, system complexity and reduce power consumption of mobile, handheld objects. Devices other than CMOS can be co-integrated with CMOS to interface the outside Multiphysics world (MEMS, sensors and actuators, RF devices, power devices,…) allowing new functionalities. 3D Wafer Level Packaging and System on a Wafer allow these new routes.

2. Nanoelectronics scaling and use of the 3rd dimension to continue Moore's law.

The struggle for increased device performance and reduced power consumption is still the main paradigm in continuation of integration density increase[1]. Besides HiK dielectric, Thin Film FDSOI is an important option for Ultimate CMOS to master electrostatics, matching variability, leakage currents, power consumption [2,3,4,5] (Fig.1). The multigate and Gate All Around architectures maximize the Ion/Ioff ratio with the possibility to tune Ion by stacking channels or Nanowires in 3D [6, 7, 8, 9] (Fig. 2). Stacked Nanowires are alternatives to linear scaling of Flash Memories in 3D [6, 10]. Stacking devices in 3D stratas through Wafer to Wafer bonding [11,12,13] allows Ge channels pMOS cold end processing on top of Silicon channels nMOS (Fig. 3) leading to substantial area reduction [12, 13].

3. Interfacing the Multiphysics World (More Than Moore) thanks to functional diversification.

The connection of Nanoelectronics to the outside Multiphysics world requests the use of devices with diversified functionalities such as selective sensing, actuation, imaging and displaying, power generation through available electrical, mechanical, ultra narrow band RF and High Frequency, photonic signals[1] to address societal needs (health, energy, security, communications, transport). The Heterogeneous association of so called More Than Moore type devices with CMOS nano-devices opens new applications fields. For example(Fig 4 a,b,c), resonators can be used for mass detection for chemical and bio sensors [14,15], switches for power management, RF nano-resonators for time reference, mechanical memories,…Unique opportunities exist to apply these devices to molecular level gas or liquid detection(Fig 4). Packaging and complete system design are main topic to be addressed on these devices as their properties have to be kept in the environment they interact with(Fig 4d)[16]. Mobile communications will require highly integrated, High Performance and Low Power consumption RF Front-End technology and design such as LNA, switches, ultra narrow band filters[17], passive devices.

4. Building new systems and their packaging with a 3D tool box at a wafer level.

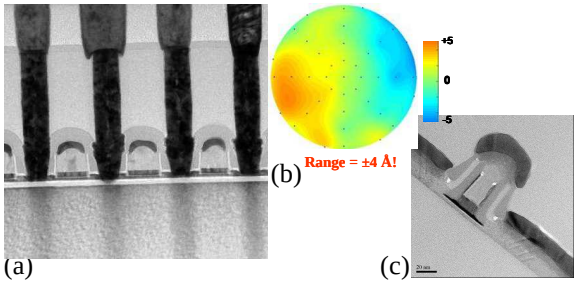
Increasing packing density and offering new functionalities on ICs is possible by co integration or 3D approaches. Efforts at LETI [16,18,19] are focused on the development of a 3D toolbox ranging from mid density TSV- i.e. Imagers like [16,18]- to Ultraflat 3D(Fig 5). Wafer Level 3D integration and Packaging (3D WLP), with shortly interconnected ultra-compact systems is possible at a reasonable cost. Low pitch Cu/Cu connections and self alignment by bonding contribute as unique options [19,20] (Fig4d). It will be possible to build Systems-On-Wafer[18] (Fig. 6), resulting from heterogeneous integration of mixed functional subsystems[21] interconnected at the wafer level [18], further using electronic, RF, optical,…signals.

5. Conclusions

Functional diversification added to Nanoelectronics will make possible new future systems to address increasing societal needs. 3D integration will address, at the wafer level, device to packaging technologies capable of reducing cost and improving system performance.

References

[1] ITRS 2009
[2] C.Fenouillet et al, *VLSI Tech Symp*, p. 65,(2010)
[3] O.Weber et al.,*IEDM*., p.176,(2008)
[4) F.Andrieu et al, *VLSI Tech Symp*, p. 57, (2010)
[5] V.Barral et al, *IEDM*., p61, (2007)
[6] T.Ernst et al. , *IEDM*, p745-748, (2008)
[7] E.Bernard et al., *VLSI Tech Symp*., p16,(2008).
[8] C.Dupré et al., *IEDM 2008*,p748-751
[9] K.Tachi et al., *IEDM*, p.313, (2009)
[10] A.Hubert et al, *IEDM*, p.637, (2009)
[11] M.Vinet et al., EDL, ,5, p.317, (2005).
[12] P. Batude et al., *IEDM*, pp346, (2009)
[13] P. Batude et al., *VLSI Tech Symp*., p.166,(2010).
[14] L. Duraffourg et. al, APL 92, 174106 (2008)
[15] E Mille et al, Nanotechnology, 165504, (2010)
[16] G.Poupon et al., Proc IEEE, pp. 60-69, (2009
[17] A. Volatier et al., *Ultrasonics Symp*, p. 902, (2005).
[18] N. Sillon et Al , *IEDM*, p595-597, (2008)
[19] P.Leduc et al, *IEEE 3DIC*, pp 1-5, (2009)
[20] T. Fukushima et al, *IEEE ECTC*, (2007)
[21] JISSO Roadmap 2008



(a) (b) (c)

Fig 1 Ultra Thin BOX and ultra thin FDSOI have been demonstrated (a) TSi=8nm; TBOX=10nm Lg=40nm on 300 mm wafers (b) Mapping of SOI thickness on 300mm substrates achieved by Smartcut; (c)Strain can be controlled on 3.5 nm SOI channel Lg=18nm [2,3,4,5]

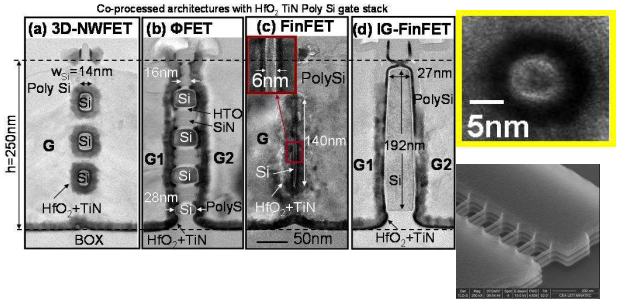
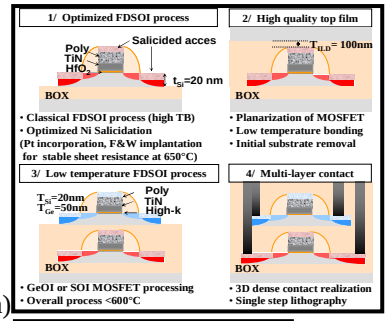
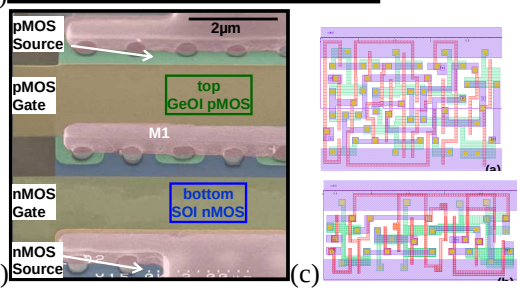


Fig 2 Tunable shaped nanowires can be 3D stacked from a top down process approach. Record Ion(13mA/µm) and Ioff (6pA/µm) MOSFETs can be obtained [6, 7, 8 ,9]. It is possible to make Gate All Around, parasitic gate capacitance minimized, FinFET. 3D High Density NAND Flash Memory[10] can be integrated. All architectures allow independently biased gates.

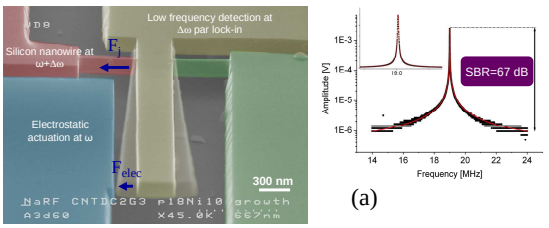


(a)

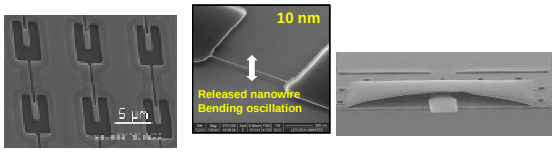


(b) (c)

Fig 3. 3D sequential integration of elementary function: (a) bottom access salicidation and Wafer Bonding. (b)HP/ LSTP options are addressed by top p-MOSFET in GeOI/hybrid orientation Si. (c) 40% gain in standard cells layout is obtained[12,13]

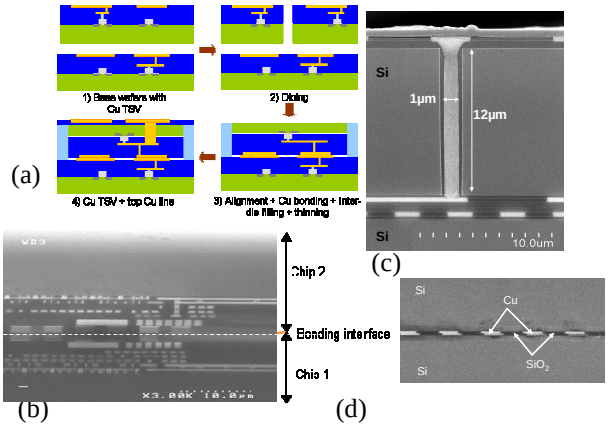


(a)



(b) (c) (d)

Fig. 4. CMOS co integratable Silicon MEMS (a) resonator for High resolution Mass Piezo resistive detection. by NEMS[14,15]; (b) NEMS arrays will increase detection sensitivity; (c) 10 nm Nanowire can improve resolution down to less than 0.3zg[6] using the same process as in Fig 2; (d) Wafer level Packaging and 3D integration apply to Above IC MEMS/NEMS [16]



(a) (b) (c) (d)

Fig. 5. Examples of: (a) ultraflat 3D process flow (die to wafer); (b)Demonstration of Oxide-Oxide bonding on CMOS wafers. Self assembly has been demonstrated. (c)Use of 3D High Density TSV to increased System compactness; (d) Cu/Cu bonding [18,19,20]

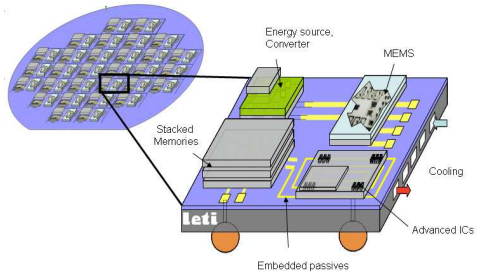


Fig 6 System On Wafer: All silicon approach for heterogeneous integration. Active silicon interposer Technology make Several functions in one single package possible[16,18]

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