

InAlN/GaN HEMTs: Recent Progress and Challenges for the Future

Ján Kuzmík

Inst. of Electrical Engineering, Slovak Academy of Sciences, Dúbravská cesta 9, 841 04 Bratislava, Slovakia
and Advanced Materials and Device Analysis Group, TU Vienna, A-1040 Vienna, Austria
Phone: +421 2 5922 2363 E-mail: Jan.Kuzmik@savba.sk

1. Introduction

Development of high-power III-nitride electronics is historically based on the AlGaN/GaN system [1]. The heterointerface quantum well (QW) junction exhibits fixed polarization charge arising from the difference ΔP_0 in spontaneous polarization of the two materials and from the strain-related piezoelectric field P_{piezo} in the barrier layer. To enhance the HEMT power performance further and to facilitate nanometer-scale gate length devices it is necessary to scale down the barrier layer thickness and simultaneously to increase the two-dimensional electron gas density (n_{2DEG}) by increasing the total polarization. Thus to scale down the device, increasing the strain in the barrier layer by using a higher amount of Al in the AlGaN seems to be the most effective way. However, serious obstacle for this idea is represented by a possible relaxation of the barrier layer. On the other hand, if we replace AlGaN with InAlN, the strain in the barrier layer can be minimized and reaches zero for $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ lattice-matched to GaN [2]. Moreover it was shown that for $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$, n_{2DEG} induced by ΔP_0 alone is about twice as much as for the conventional $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ and reaches $2.7 \times 10^{13} \text{ cm}^{-2}$ [3].

2. State-of-the-art InAlN/GaN HEMTs

DC testing and output characteristics of InAlN/GaN HEMTs confirmed superiority of this novel approach. With $0.25 \mu\text{m}$ gate length the highest maximum drain current was 2.3 A/mm at room temperature, and above 3 A/mm at 77 K , even on the sapphire substrate [4]. Moreover, it has been shown that InAlN/GaN HEMTs can operate during heating at $1000 \text{ }^\circ\text{C}$ without any permanent damage [4]. This may be the highest operational temperature of any solid-state device. No strain in the structure and a ceramic-like property of InAlN compound may account for that.

In terms of RF performance of InAlN/GaN HEMTs outstanding values were reported for current gain cutoff frequency $f_T = 205 \text{ GHz}$ [5], elsewhere large-signal parameters reached 10 W/mm and 50% PAE at 10 GHz [6] or 5.8 W/mm at 35 GHz [7]. We note that all these data refer to the Ga-polar devices; however N-polar InAlN-based HEMTs are also promising [8].

3. Towards normally-off and highly reliable InAlN/GaN HEMTs

InAlN/GaN HEMTs with only 2 nm barrier capped with

highly doped n^{++} GaN have been proposed to obtain the enhancement mode device [9,10]. Selective etching of the cap layer resulted in the well-controllable ultrathin barrier device with threshold voltage of $V_T > 0.4 \text{ V}$. The n^{++} GaN layer eliminated current dispersion without additional surface passivation, see Fig. 1(b). Normally-off devices with the gate length of $0.25 \mu\text{m}$ and $4 \mu\text{m}$ source-to-drain distance exhibited maximum current of 0.8 A/mm , maximum transconductance of 400 mS/mm and cut-off frequency 50 GHz [10]. Annealing of the normally-off

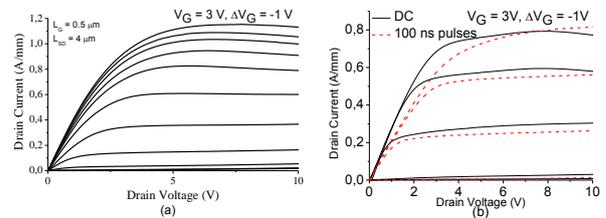


Fig.1 DC and pulsed output characteristics of (a) the normally-on InAlN/GaN and (b) the normally-off InAlN/GaN HEMTs processed on the same epi-wafer.

InAlN/GaN HEMTs at $500 \text{ }^\circ\text{C}$ for 2 minutes increases the transconductance to 650 mS/mm and the threshold voltage becomes even more positive [11]. In addition, depletion mode MOS HEMT devices on the same wafer have been demonstrated by applying the gate insulation, see Fig. 1(a), opening up a good perspective for reproducible high-performance InAlN-based digital integrated circuits [9,10].

Degradation tests have been performed on lattice-matched InAlN/GaN HEMTs using either high negative gate bias (NGB) stresses, or semi-on stresses or off stresses [12]. The drain current decrease observed after consecutive NGB stresses was explained by the access resistances increase; however the parameters could be fully recovered. This was in contradiction to earlier reports on AlGaN/GaN HEMTs where similar NGB experiments lead to the excessive inverse piezoelectric effect causing destructive damages [13]. Thus the lack of the strain in the InAlN/GaN HEMT barrier may mitigate piezoelectric destruction mechanism. On the other hand, by comparing all the stress conditions, the highest vulnerability of the InAlN/GaN HEMTs has been observed for off-state stress conditions [12], while in this case AlGaN/GaN HEMTs seem to be less vulnerable [13]. Thus hot-electron effects in the GaN buffer seem to be pronounced for InAlN/GaN HEMTs [12]. This is probably because of the thin InAlN barrier, which results in higher vertical electrical fields

under the gate if compared with AlGaIn/GaN HEMTs. However it was shown that hot electrons may be blocked by using a double-heterostructure QW in InAlN/AlN/GaN/AlGaIn/GaN HEMTs [14].

4. Towards THz frequency HEMTs

An ensemble Monte Carlo simulation of a non-polar InAlN/InN/InAlN HEMTs has predicted f_T of more than 1 THz for a gate length of 50 nm [15]. This was due to extremely high drift velocity in InN channel [15]. Later it was suggested that polar InAlN/InN-based HEMTs

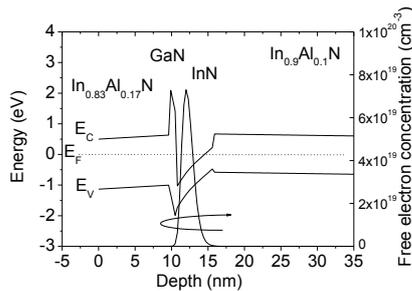


Fig. 2 Energy band gap diagram and free electron concentration profiles for cation polarity $\text{In}_{0.83}\text{Al}_{0.17}\text{N}/\text{GaN}/\text{InN}/\text{In}_{0.9}\text{Al}_{0.1}\text{N}$ HEMTs.

may be also realized by inserting a thin GaN spacer between the InN channel and InAlN barrier [16]. The spacer may be necessary to confine the carriers in the channel, see Fig. 2, and also be beneficial for the high electron mobility. It was emphasized that managing of the semi-insulating InAlN buffer and/or gate processing are among the major challenges to be solved before the device becomes feasible.

5. Conclusions

InAlN/GaN HEMTs have demonstrated the record drain current density (up-to 3 A/mm), extreme thermal stability (up-to 1000 °C environmental temperature) and scalability (having only 2 nm barrier thickness). The gate recessing through highly doped GaN cap layer lead to the regime of the normally-off InAlN/GaN HEMT. 0.25 μm gate-length InAlN/GaN HEMT with $V_T > 0.4$ V has demonstrated excellent small signal *rf* parameters ($f_T = 50$ GHz), which can be further improved with shorter gate length and source-to-drain distance, respectively. Analysis of the degradation mechanism in InAlN/GaN HEMTs excluded inverse piezoelectric effect to cause the damage, which proved the prospect of the increased durability of the lattice-matched devices. The InAlN/GaN/InN/InAlN HEMT concept is promising for a break-through into the THz frequency range.

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