

Improvement of Current Collapse in Deeply Recessed Gate AlGaIn/GaN High Electron Mobility Transistors without Field Modulating Structure

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1. Introduction

GaN-based high electron mobility transistors (HEMTs) are attractive for devices that require high power operation at high bias voltage. However, the performance of the GaN HEMTs has been limited by direct current to radio frequency (DC-RF) dispersion (i.e. current collapse) [1]. It is widely known that current collapse can be effectively reduced by the reduction of surface states locating in the gate drain access region by SiN_x passivation [2] and/or the modulation of electric field at the gate edge by field plate structure [3]. However, a field modulating structure is undesirable because its intrinsic gate capacitance tends to degrade the devices' performance at the higher frequencies. A recessed gate structure is also reported to have an effect of reducing current collapse [4]. So, in order to balance a lower intrinsic gate capacitance with reduction of current collapse, a recessed gate structure without any dielectric is necessary to satisfy both high frequency and high bias voltage operation.

In this article, we report our investigation of the variation of intrinsic gate capacitance depending on the presence or absence of a dielectric film, and the relationship between the recess depth and the influence of field modulation on drain current.

2. Experimental

The AlGaIn/GaN HEMT structures employed in this study are schematically shown in Fig. 1. The epitaxial layers were grown on a semi-insulating SiC substrate by using metal organic chemical vapor deposition (MOCVD) technique. The device structures consisted of GaN channel, 15 nm-thick AlGaIn barrier (28% Al composition), and a GaN cap layer (0-200nm). After MOCVD growth, ²⁸Si ions were selectively implanted at room temperature. In addition, implanted Si ions were activated by rapid thermal annealing. After fabricating the source/drain ohmic contacts of Ti/Nb/Pt and implant isolation, we deposited SiN as a passivation by catalytic chemical vapor deposition (cat-CVD) and SiO₂ as a dielectric film for field modulation by plasma-enhanced chemical vapor deposition (PECVD). Lastly, we fabricated recessed gate structures. The gate recess etching was performed by an inductively coupled plasma (ICP) etching system with a SiO₂ dielectric film as a

mask. In this study, four thicknesses of GaN cap layers (20, 50, 100, and 200nm) were used to precisely control recess depth by selective etching stop technique at the interface of AlGaIn barrier layer, so the recess depth was equal to the GaN cap thickness. After the gate recess etching, the Ni/Au gate electrodes were deposited by electron-beam evaporation and lift-off technique.

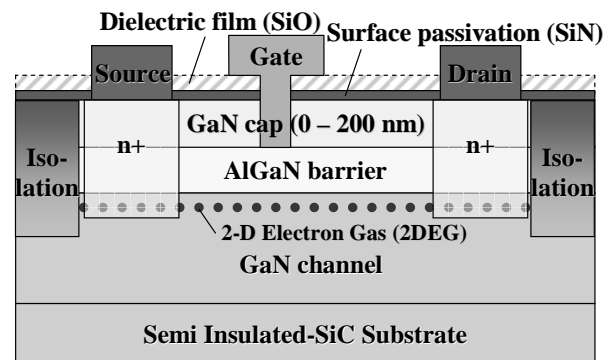


Fig. 1 Schematic structures of HEMTs with a recessed gate structures.

We measured DC current-voltage (I-V) characteristics and small-signal characteristics of the HEMTs which had 1.0 μm gate length, 100 μm gate width and a distance of 3.0 μm between gate and drain electrode. The intrinsic parameters were extracted by small-signal analysis, and the variation of intrinsic gate capacitance associated with or without a dielectric film was investigated. We also estimated the relationship between recess depth and the impact of drain current collapse from the drain current ratio of pulsed operation to DC operation at the drain bias voltage of 5 V.

3. Results and Discussion

Figure 2 shows the variation of a gate-drain capacitance of the HEMTs with/without dielectric films. We extracted gate-drain-capacitance from the data of small-signal measurements. For both a planar gate HEMT (non-recessed gate HEMT without a GaN cap layer) and a recessed gate HEMT, the removal of the dielectric film reduced the gate-drain-capacitance by about 15%.

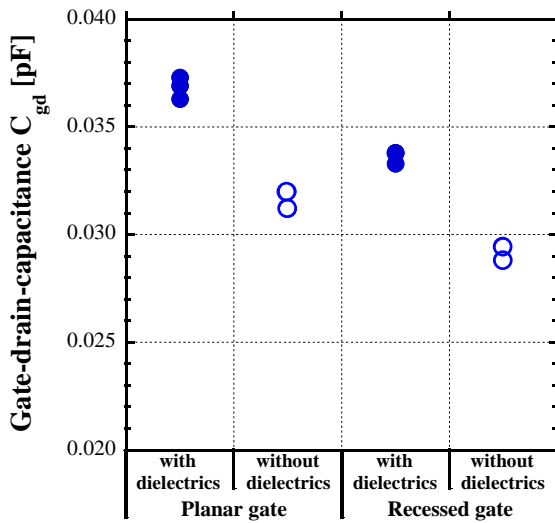


Fig. 2 The variation of a gate-drain-capacitance of the HEMTs with/without SiO dielectric film.

Figure 3 shows the relationship between recess depth (GaN cap thickness) and the drain current ratio of pulsed operation to DC operation (drain current RF/DC ratio). The devices with SiO film showed an almost constant drain current ratio at any recess depth. The result indicated that the field modulating structure effectively improved drain current collapse, so the effect of the recessed gate structure was obscured. On the other hand, the drain current ratio of the devices without SiO film depended on recess depth. For the planar gate HEMT, the removal of SiO film quadrupled the amount of drain current reduction. However, the amount of drain current reduction decreased with an increase of recess depth. Finally the amount of drain current did not depend on whether the SiO film was removed or not at a GaN cap thickness of 200 nm. On the basis of the results, the recess depth of over 200 nm was required in order to obtain HEMTs whose drain current collapse was suppressed well.

From these results, we found that adoption of deeply recessed gate HEMTs enabled the reduction of gate capacitance without current collapse. Therefore, it is expected that a power added efficiency (PAE) increased with increasing a drain current RF/DC ratio (i.e. improvement of drain efficiency). According to our previous experiences, the above reduction of capacitance is estimated to correspond to about 1dB improvement of available power gain.

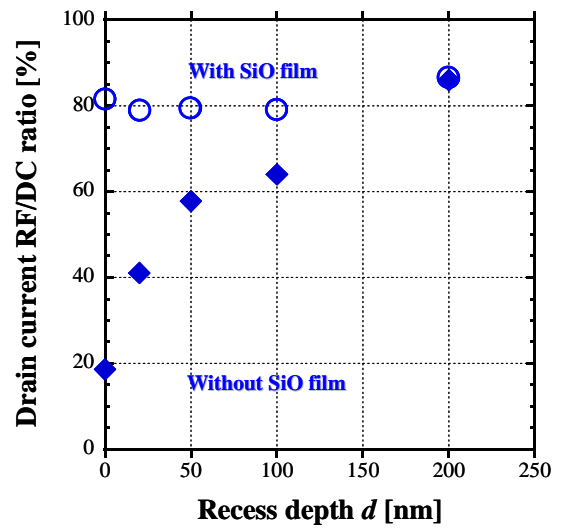


Fig. 3 The relationship between recess depth and the drain current ratio of pulsed operation to DC operation.

4. Conclusion

We investigated the variation of intrinsic gate capacitance depending on the presence or absence of a dielectric film, and assessed the influence of recess depth on the drain current RF/DC ratio. We clarified that the drain current RF/DC ratio of the HEMTs without dielectrics increased with an increase in the recess depth, while that of the HEMTs with dielectric film was independent of the recess depth. Under our experimental conditions, our results indicate that recess depth needs to be at least 200 nm to be equal in drain current RF/DC ratio to field modulating structures.

According to the result of the intrinsic parameter extraction, gate-drain-capacitance was reduced about 15% by removing dielectric film. This indicates that a deeply recessed gate structure is highly-promising for use in high frequency operation.

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References

- [1] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices, **48** (2001) 560
- [2] Greene BM, Chu KK, Chumbes EM, Smart JA, Shealy JR, and Eastman LF, IEEE Electron. Dev. Lett., **21** (2000) 268.
- [3] Y.Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara IEEE Electron. Dev. Lett., **24** (2003) 289.
- [4] R. Chu, L. Shen, N. Fichtenbaum, Z. Chen, S. Keller, S. P. DenBaars, and U. K. Mishra, IEEE Electron. Dev. Lett., **29** (2008) 303.