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Effects of Plasma-PH_3 passivation on Mobility Degradation Mechanisms and Current Conduction Mechanisms of $In_{0.53}Ga_{0.47}As$ N-MOSFET

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1. Introduction

III-V compound semiconductor is becoming attractive as a material for high performance MOSFETs. In fact, the high performances of InGaAs MOSFETs with plasma-PH_3 passivation treatment have been demonstrated and the effect of variable process parameters have been studied [1-2]. Improvements made by the treatment is due to the presence of P-for-As exchange reaction through removal of As-O_x components and the P_xN_y layer which achieves an abrupt, smooth interface. However, understanding of how this treatment is effective in improving the device performance in terms of its mobility (μ) and current conduction have yet to be understood, especially since a detailed knowledge of carrier transport can give insight to defects that are present in the oxide. This motivated our current work.

2. Device Fabrication

MBE grown $In_{0.53}Ga_{0.47}As$ on InP substrate was processed for device fabrication and material characterization. Detailed process flow can be referred to in Ref [1-2]. However, this work uses HfAlO of 5nm thick. After device fabrication, devices were measured at a temperature range between 250K to 420K for analysis.

3. Mobility Scattering Mechanisms & Factors causing Mobility Improvement

To investigate the factors governing μ, temperature dependence was investigated shown in Fig 1. μ of non-passivated devices, with interface trap correction, shows that at low $E_{eff,}$ it increases with decreasing temperature, but still weaker than that of plasma-PH_3 passivated. This means that Coulombic scattering, which partially hides the effects of scattering with high-k phonons, contributes to the μ for non-passivated devices. However, phonon scattering contributes to μ of plasma-PH_3 passivated. Under high E_{eff}, μ is weakly dependent on temperature for non-passivated, but still strongly dependent on temperature for plasma-PH_3 passivated, suggesting surface roughness scattering or interface dipole scattering for the former and phonon scattering for the latter. However, RMS data from AFM shows ~0.16nm and ~0.15nm for non-passivated and plasma-PH_3 passivated respectively, with TEM images shown in Fig 2 (a) and (b) not revealing any significant increase in interface roughness, deduced from the waviness of the interface. This shows the possibility of interface dipole scattering in the non-passivated devices.

Since electron trapping induced by charges near the conduction band edge (E_c) could be the cause for low channel μ of MOSFETs, the reduced D_{it} values near E_c for passivated devices may be the reason for the improvement in the low E_{eff} μ. Close to one order of magnitude reduction in D_{it} near to E_c as shown in Fig 3 is observed due to the ability of the passivation in reducing elemental As and As-As bond which have their energy levels in the upper half of the bandgap [3-4]. This may be achieved by forming volatile hydrides, AsH_x [2], through the small amount of H atoms existing in the PH_3-based plasma treatment process and P-for-As exchange reaction. It can also be effective in reducing Ga vacancies seen in the reduction in D_{it} at ~0.2eV above E_v [5] which is also confirmed from Ga outdiffusion into the high-k from EDX (not shown). Fixed oxide charges gives values 0.75-2.2x10^{11}cm^{-2} for passivated and non-passivated respectively, which is one order lesser than that of D_{it} implying that a significant amount of Coulombic scattering is caused by D_{it}. For the mid E_{eff} region, a more severe phonon scattering for non-passivated compared to passivated is observed, based on μ_{ph} results from Matthiessen's rule. Phonon scattering from the substrate is expected to be the same for both samples, and hence the existence of the additional source of phonon scattering from the non-passivated suggests that HfAlO/$In_{0.53}Ga_{0.47}As$ interface contributes to an interfacial phonon scattering which is suppressed by the presence of the P_xN_y layer. The origin of this scattering, caused by the soft optical phonons in HfAlO, was found to have its scattering rate having a relatively weak function of temperature (not shown). Finally, the interface dipole scattering that exists at high E_{eff} of non-passivated could be due to Hf atoms (smaller electronegativity than Al) occupying the Ga vacancy sites, which changes the polarity of the interface dipoles, hence enhancing the potential fluctuation at the interface as explained in [6].

4. Current Conduction Mechanisms

Gate current density result shows that plasma-PH_3 passivation is seen to improve, not only the μ characteristics, but also the current density voltage. The curves of Fig 4, obtained from substrate injection region, are in agreement with Lampert's Space Charge limited Conduction (SCLC) theory. At 300K and low E_{eff}, the curves are linear with slopes ~1, indicating an Ohmic behavior. However, a larger contribution of Ohmic conduction current is observed in non-passivated than passivated devices due to the higher D_{it} existing near the E_c (shown in Fig 3) with the shallower traps lying closer to E_c, thus generating a hopping current [7]. Beyond Ohmic region, Fig 4(a) shows non-passivated devices experiencing a slope of ~3.05 in the J-V equation [8] which implies the trap states being exponentially distributed in energy [9]. This could originate from surface defects like vacancies and structural disorders, which could also be responsible for the interface dipole scattering explained earlier. On the other hand, Fig 4(b) shows that plasma-PH_3 passivated device does not have a slope of at least 2, thus it does not experience an SCLC regime, but only Ohmic conduction dominates at 300K implying that carrier transport is facilitated through the oxide. At >300K, Fig 4(a) shows the absence of Ohmic conduction in the low E_{eff}, since the slopes deviate from ~1. However the presence of Schottky emission (not shown) suggests it would be more appropriate to consider the leakage behavior of non-passivated devices as being controlled by Frenkel Poole emission and not SCLC at high E_{eff}. The trap energy levels are given as ~0.47-0.54eV below E_c. On the other hand, the slopes of ~2 for plasma-PH_3 passivated devices in Fig 4(b), imply a trap-free SCLC regime, where injection of carriers at the interface is limiting the current hence indicating a well formed interface between HfAlO and InGaAs.

5. Summary

Carrier transport mechanisms of non-passivated and plasma-PH_3 passivated InGaAs MOSFETs have been studied with temperature dependence. It is found that Plasma-PH_3 passivation improves the device performance through (i) reduction in D_{it} resulting in reduced Coulombic scattering at low E_{eff} (ii) reduced surface optical phonon scattering at mid $E_{eff,}$ and (iii) reduced interface dipole scattering at high E_{eff}. Also, the dominance of Ohmic conduction and trap-free SCLC mechanism at >300K, in comparison to Schottky emission and Frenkel Poole emission (trap energy levels~0.47-0.54eV) for non-passivated, at low E_{eff} and high E_{eff} respectively, is the cause of reduced gate leakage and also imply the improvement in interface quality. The origins of the defects contributing to these conduction mechanisms could be related to the increased Coulombic scattering at low E_{eff} and interface dipole scattering at high E_{eff} for non-passivated devices.

References

[1] J.Q.Lin *et al*., *Tech .Digest IEDM ,* (2008), 977
[2] H.-J.Oh et al, *J. Electrochem.Soc*.,**157**, (2010), H1051
[3] G.Brammertz et al, *J. Electrochem.Soc* **155,**(2010), H945
[4] J.Robertson,*Microelectronic Eng*. **86**, (2009), 1558
[5] H.P.Komsa, *Microelectronic Eng*., **88**, (2011), 1436
[6] Y.Urabe *et al*, *Tech .Digest IEDM* , (2010), 142
[7] P. Mark *et al*, *J. Appl. Phys*. **33**, (1962), 205
[8] D. Joung et al, *Appl.Phys.Lett,* **97**, (2010), 093105
[9] R.Perera *et al*, *Microelec.Eng*., **65**, (2003), 357

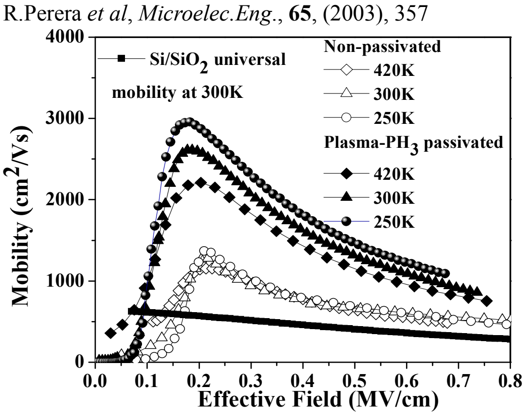

Fig 1. Effective electron mobility in non-passivated and pasivated InGaAs N-MOSFETs at various temperatures from 250K to 420K

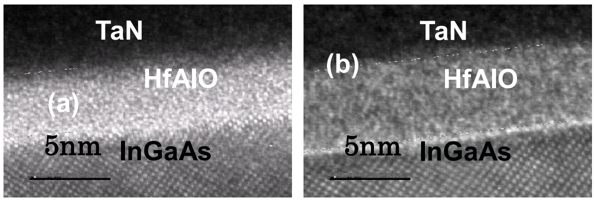

Fig 2(a) HR-TEM images of non-passivated and (b) plasma-PH_3 passivated InGaAs MOSFET.

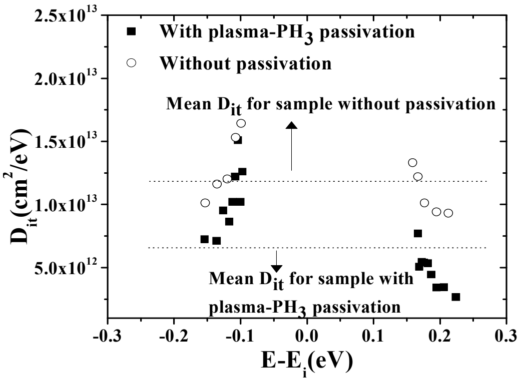

Fig 3. Energy distribution of D_{it} as determined by the rise/fall time dependence of Charge Pumping currents. ~Two times reduction in mean D_{it} is observed with plasma-PH_3 passivation compared to non-passivated.

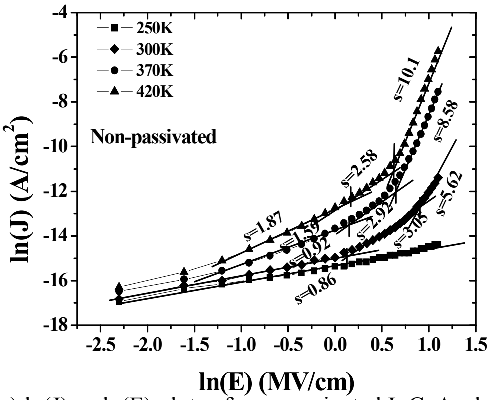

Fig 4 (a) ln(J) vs ln(E) plots of non-passivated InGaAs devices for temperatures between 250K to 420K.

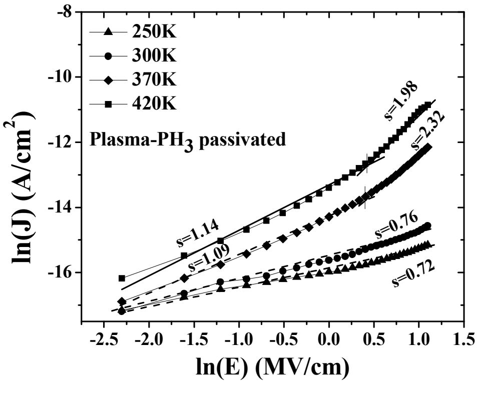

Fig 4 (b) ln(J) vs ln(E) plots of plasma-PH_3 passivated InGaAs devices for temperatures between 250K to 420K.