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$In_{0.53}Ga_{0.47}As$ Channel N-MOSFETs with Shallow Metallic S/D Extension

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ABSTRACT

We report the first demonstration of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with a shallow metallic source/drain extension (SDE). A SDE-last process was used: the Ni-InGaAs metallic SDE was formed last, after deep n^+ S/D implant, to achieve self-aligned highly-abrupt SDE junctions. Junction leakage between was effectively suppressed by ~40 times with the deep S/D implant.

INTRODUCTION

InGaAs n-MOSFETs could potentially replace Si n-MOSFETs for logic applications in sub-16 nm technology node [1]-[7]. InGaAs MOSFETs are more vulnerable to short channel effects (SCE) than Si MOSFETs due to the narrower bandgap and higher permittivity of InGaAs material. Therefore, SCE control in InGaAs MOSFETs is important. Various S/D junction engineering techniques has been shown to reduce SCE, such as ultra-shallow junction formation and anti-punchthrough halo (pocket) implantation [8]-[9].

In this paper, InGaAs MOSFETs with shallow and highly-abrupt metallic SDE were proposed for reduction of SCE. The metallic SDE formation comprises of Ni reaction with InGaAs and selective etch of unreacted excess Ni. A SDE-last process was developed to realize this novel structure.

DEVICE FABRICATION

Fig. 1 shows the process flow for fabricating an $In_{0.53}Ga_{0.47}As$ N-MOSFET with Ni-InGaAs shallow SDE and deep S/D implant. Key steps are schematically illustrated in Fig. 1(b).

$In_{0.53}Ga_{0.47}As$ (thickness of 1 μm, p-type doped at 2×10^{16} cm^{-3}) on p^+ InP substrates were used for device fabrication. After pre-gate clean, and *ex situ* passivation using $(NH_4)_2S$, the sample was quickly loaded into an atomic layer deposition (ALD) tool for Al_2O_3 deposition. Post-gate dielectric deposition anneal (PDA) at 400 °C for 60 s was then performed using rapid thermal anneal (RTA). This was followed by the TaN gate electrode deposition and gate stack patterning. Silicon oxynitride (SiON) spacer was formed before deep S/D Si implantation (20 keV, 1×10^{14} cm^{-2} dose). SiON spacer was removed after a 600°C 60 s dopant activation.

15 nm Ni was sputtered over the whole wafer. A RTA at 250 °C for 60 s was carried out to induce reaction between Ni and InGaAs, forming the Ni-InGaAs S/D extension. Selective etch of unreacted excess Ni using concentrated HCl was done to complete the device fabrication. The Ni-InGaAs serves as both SDE and S/D metal contact.

RESULTS AND DISCUSSION

Cross-sectional TEM images of a device structure with SiON spacer formed before deep S/D implant are shown in Fig. 2. Fig. 3 shows the TEM image of a completed $In_{0.53}Ga_{0.47}As$ n-MOSFET with shallow Ni-InGaAs SDE. Ni-InGaAs extension as shallow as sub-10 nm can be achieved by precise control of the sputtered Ni thickness.

The reaction between Ni and InGaAs involves diffusion of Ni into InGaAs. This enables the integration of Ni-InGaAs SDE. An atomic composition of Ni: In: Ga: As = 43: 12: 16: 29 was detected in the Ni-InGaAs SDE region by energy dispersive X-ray spectroscopy (EDX). Lateral diffusion of Ni-InGaAs under the gate stack was observed. Secondary ion mass spectrometry (SIMs) analysis at the S/D contact region is shown in Fig. 4. The profile of Ni and Si shows that thin Ni-InGaAs layer was formed above the deep S/D implant Si concentration peak position.

I_D-V_G, I_D-V_D, and extrinsic transconductance $G_{m,ext}$ -V_G plots for a device with 5 μm gate length and 2.5 nm EOT are shown in Fig. 5, 6, 7, respectively. Good transfer and output characteristics were observed. Significant performance enhancement can be expected when integrating this novel structure into short channel device with lower EOT.

I-V characteristics of the source-to-body junction of n-MOSFETs with Ni-InGaAs SDE were measured. Similar measurements were performed on devices with Ni-InGaAs directly formed on p-InGaAs (as illustrated in Fig. 9). The cumulative probability plot shown in Fig. 8 compares the leakage current density taken at the reverse bias of 1 V. Around 40 times reduction of reverse leakage current density was achieved with the deep S/D implant.

Table I compares our proposed novel metallic SDE junction structure with other three different S/D junction structures. MOSFETs with thick Ni-InGaAs contact formed on implanted n type S/D can significantly suppress the off-state leakage current compared to MOSFETs with Ni-InGaAs formed directly on p type InGaAs [10]-[11]. Shallow Ni-InGaAs SDE formed last may be promising for reduction of DIBL in short channel InGaAs MOSFETs. Compared with the conventional short channel devices with lightly doped S/D extension, the novel Ni-InGaAs SDE can achieve a more abrupt SDE junction.

CONCLUSION

InGaAs n-MOSFETs featuring Ni-InGaAs SDE was proposed and demonstrated by using the SDE-last process for the first time. The deep S/D implant suppresses the source to drain leakage current. Accurate control of the SDE junction abruptness make this novel structure a promising candidate for extremely small scale InGaAs MOSFETs.

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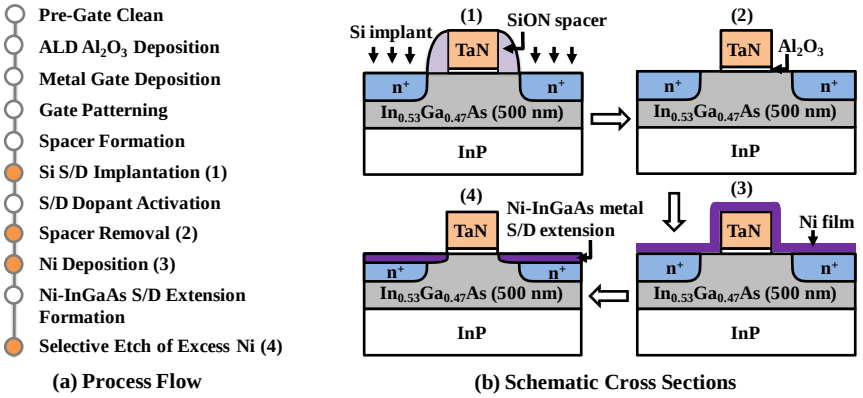

Fig. 1. (a) Process flow for $In_{0.53}Ga_{0.47}As$ n-MOSFETs with a novel Ni-InGaAs S/D extension; (b) Schematics illustrating device cross-sections after various fabrication steps: (1) Si S/D implant, (2) Spacer removal, (3) Ni deposition, and (4) Selective etch of excess Ni.

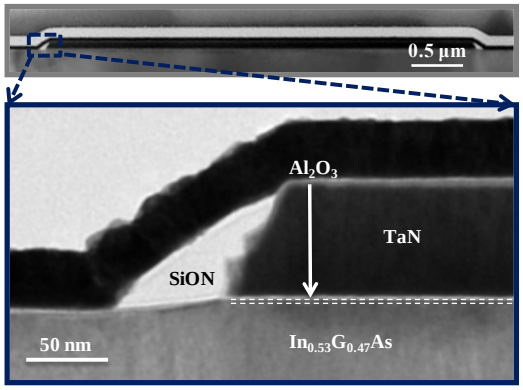

Fig. 2. TEM micrographs showing a device structure with SiON spacers formed before deep S/D implant.

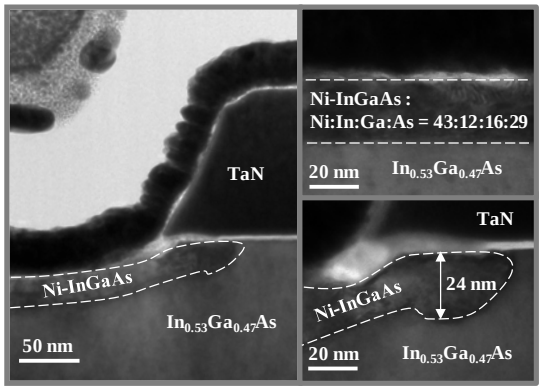

Fig. 3. TEM micrographs of a completed $In_{0.53}Ga_{0.47}As$ n-MOSFET with novel Ni-InGaAs S/D extension.

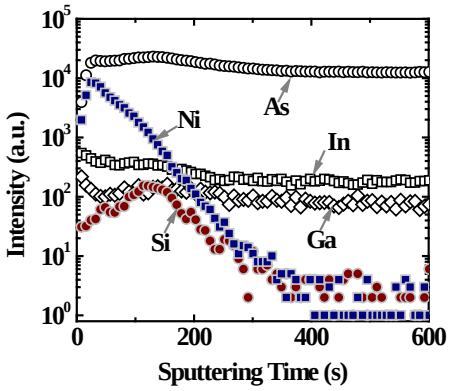

Fig. 4. Profile of Ni, In, Ga, As and Si in source area with Ni-InGaAs S/D extension formed on n^+ InGaAs, obtained using Secondary Ion Mass Spectrometry.

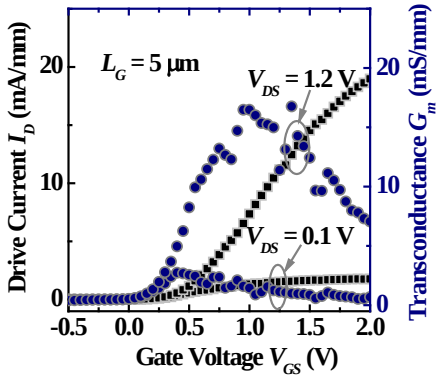

Fig. 5. I_D-V_{GS} and G_m-V_G characteristics of an $In_{0.53}Ga_{0.47}As$ n-MOSFET with novel Ni-InGaAs S/D extension.

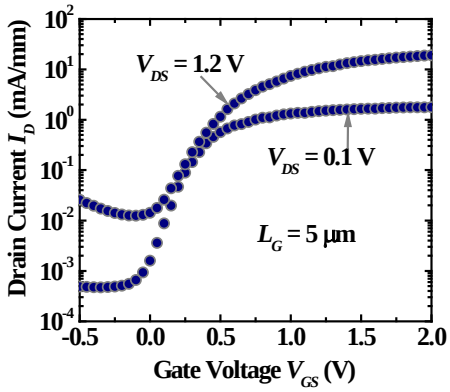

Fig. 6. I_D-V_{GS} transfer characteristics of an $In_{0.53}Ga_{0.47}As$ n-MOSFET with novel Ni-InGaAs S/D extension having SS of 134 mV/decade.

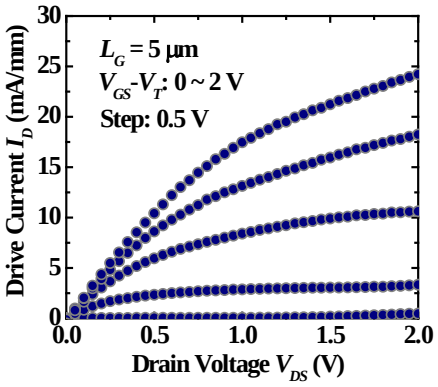

Fig. 7. I_D-V_{DS} characteristics of a $In_{0.53}Ga_{0.47}As$ n-MOSFET with novel Ni-InGaAs S/D extension.

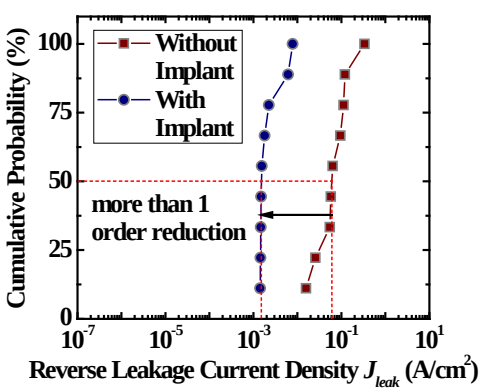

Fig. 8. Reverse Leakage Current Density J_{leak} from source to body comparison between novel $In_{0.53}Ga_{0.47}As$ n-MOSFETs with and without Si S/D deep implantation. (refer to Fig. 9).

Table I. Comparison of MOSFETs with Ni-InGaAs contact formed on p or n type InGaAs, conventional n-MOSFET with LDD and the novel n-MOSFET with Ni-InGaAs metal S/D extension as demonstrated in this paper.

MOSFET with Different Structures	n-MOSFET with Ni-InGaAs S/D Contact	n-MOSFET with Ni-InGaAs S/D Contact on n^+-InGaAs	Conventional n-MOSFET with S/D shallow Implant Extension and Deep S/D Contact Implant	Novel n-MOSFET with Ni-InGaAs S/D Extension and Deep S/D Contact Implant
Schematic Cross Sections	Ni-InGaAs, TaN, p-InGaAs	Ni-InGaAs, n^+, TaN, p-InGaAs	LDD, TaN, n^+, n^+, p-InGaAs	Ni-InGaAs, TaN, n^+, n^+, p-InGaAs
Advantages or Disadvantages	High S/D leakage current	S/D leakage current suppressed	Non-abrupt junction due to Si implantation profile tail	S/D leakage current suppressed, accurate control of junction abruptness and reduce DIBL in short channel devices

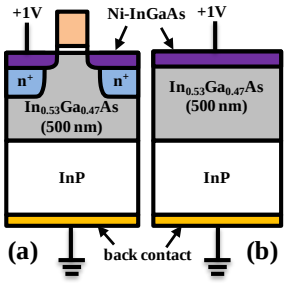

Fig. 9. Schematic illustrations of J_{leak} measuring from (a) source to body of a n-MOSFET with novel Ni-InGaAs S/D extension – blue circle data points in Fig. 8 and (b) a diode with the same Ni-InGaAs thickness directly firmed on p-InGaAs – square red data points in Fig. 8.