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GaAsSb/InGaAs Vertical Tunnel FET with a 25 nm-wide Channel Mesa Structure

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1. Introduction

The tunnel field-effect transistor (TFET) is an attractive option for low power devices because of its steep sub-threshold slope (SS) and high on/off current ratio. In III-V TFET, GaAsSb/InGaAs type-II TFET is promising from the simulation[1]. However, obtained characteristics [2] is not comparable to these by InGaAs TFET [3]. In this work, we fabricated a vertical channel TFET with at p^{++} GaAsSb / i- InGaAs junction and 25 nm-wide channel. Simulated I-V characteristics have a SS of 39 mV/dec and an on/off current ratio of 6.4×10^{7} when the equivalent oxide thickness (EOT) is 1 nm. The observed I-V characteristics had a SS of 130 mV/dec and an on/off current ratio of 1.5×10^{4} when the EOT was 4 nm.

2. Simulation

Using a WKB approximation, the band-to-band tunneling probability is calculated. The band diagram is obtained using the device simulator ATLAS, which is produced by SILVACO. The tunnel current density is calculated using the Esaki-Tsu formula. The channel width is 20 nm and the thicknesses of the p^{++}-, i-, and n^{+}-layers are all 40 nm. The channel is surrounded by a double gate. The p^{++}-layer consist of GaAsSb, whereas the i- and n^{+}-layers consist of InGaAs. Therefore, a type-II heterojunction is formed at the p^{++}-i junction. The carrier concentration of the p^{++}-layer is 3×10^{19} cm^{-3}, whereas the carrier concentration of the n^{+} -layer is 1×10^{19} cm^{-3}. The calculated EOT changes from 1 nm to 4 nm. The simulated I_D-V_G characteristics at a V_D of 0.3 V are shown in Fig. 1. The SS and the on current are estimated as 39 mV/dec and 2.7×10^{-2} A/mm when the EOT is 1nm, whereas the highest on/off current ratio is 1.6×10^{8} when the EOT is 2.5 nm.

3. Device Fabrication

To fabricate a vertical TFET, we used a process similar to the process developed for fabricating an InGaAs vertical MISFET [4]. The epitaxial structure was equal to simulated structure. To obtain a narrow mesa structure, we performed a selective undercut etching from the InGaAs to GaAsSb region [5]. Al_2O_3, which was deposited by atomic layer deposition (ALD), was used as

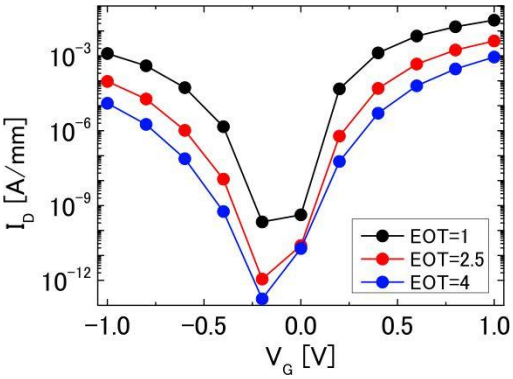

Fig. 1. Simulated I_D-V_G characteristics.

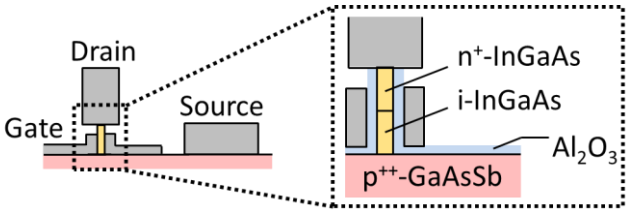

Fig. 2. Fabricated device structure.

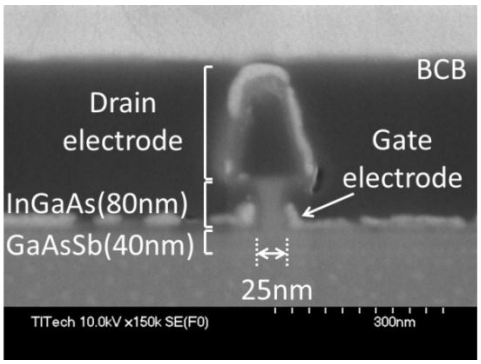

Fig. 3. SEM cross-section image of fabricated device.

a gate dielectric. The estimated EOT of Al_2O_3 was 4 nm. The schematic structure of the fabricated device is shown in Fig. 2, and the SEM cross-section image of the fabricated device is shown in Fig.3. The observed channel mesa width was 25 nm.

4. Result and Discussion

Figure 4 shows the I_D-V_G characteristics measured at room temperature. The red curve shows the characteristics of the annealed sample, whereas the black curve shows the characteristics of the sample that is not annealed. Figure 5 shows the measured I_D-V_D characteristics. The observed SS was 130 mV/dec at V_G=0.11 V and V_D=0.25 V, and the on/off current ratio was 1.5×10^4. These values are comparable to reported values by InGaAs TFET [3]. Figure 6 shows the simulated I_D-V_G characteristics at V_D = 0.3 V when the mesa width is 20 nm as well as the measured I_D-V_G characteristics at V_D = 0.25 V when the mesa width is 25 nm. Although the observed on current was almost equal to the simulated on current, the measured SS was worse than the simulated SS (57 mV/dec at EOT=4 nm). In our lateral InGaAs MOSFET with an Al_2O_3 gate insulator, the SS at V_D= 10 mV was 184 mV/dec [6] when the channel length was 170 nm. When we changed the channel length from 170 nm to 6 um, no clear change in the SS was observed. Moreover, a clear improvement in the characteristics of the MOSFET was observed as a result of annealing. Thus, we think that the degradation in the SS can be explained by the interface trap of Al_2O_3 [7].

5. Conclusions

A GaAsSb/InGaAs vertical TFET was fabricated and compared with calculated I-V characteristics. The fabricated device has a 25 nm wide mesa structure and a 4nm of EOT. The observed I-V characteristics exhibited a SS of 130 mV/dec, whereas the simulated I-V characteristics exhibited SS of 57 mV/dec when the EOT was 4 nm. This degradation in the SS can be explained by the presence of interface traps. Because the estimated SS is 39 mV/dec when the EOT is 1nm, an improvement in the gate insulator should result in an improvement I-V characteristics.

Acknowledgements

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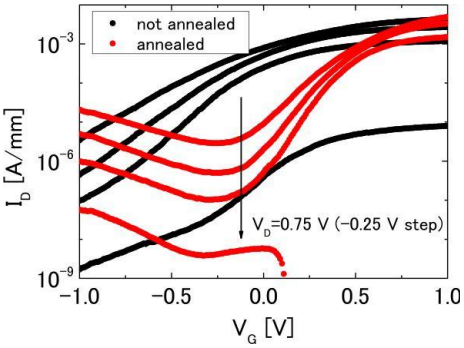

Fig. 4. I_D-V_G characteristics

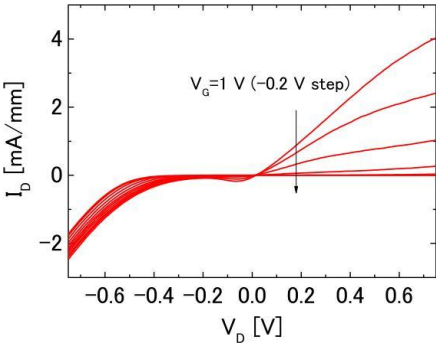

Fig. 5. I_D-V_D characteristics.

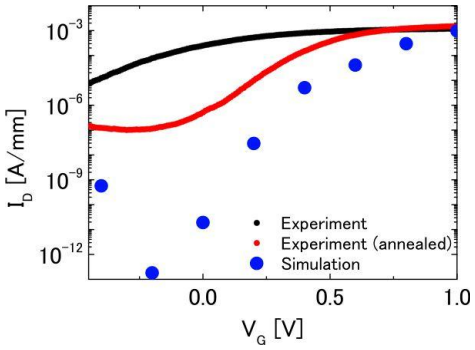

Fig. 6. Comparison between observed characteristics at V_D=0.25 V and simulated characteristics at V_D=0.3 V.