A-4-3

Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp586-587

Fluidic Self-Assembly for Heterogeneous Integration of High Performance Resonant Tunneling Diodes Using Low-Melting Point Alloy Bumps

Jun Nakano, Tomoaki Shibata, Takato Okatsu, Masayuki Mori and Koichi Maezawa

Graduate School of Science and Engineering, Univ. of Toyama
3190 Gofuku, Toyama 930-8555, Japan
Phone: +81-76-445-6725 E-mail: maezawa@ieee.org

1. Introduction

Resonant Tunneling Diodes (RTDs) have been attracting a great deal of attention for future THz devices. However, RTDs have only 2-terminals, which restricts their usage. In order to fully develop their potential it is necessary to integrate with other devices. Therefore Heterogeneous integration (HI) is a key technology to develop real RTD applications. Among them, Fluidic Self-Assembly (FSA) is one of the most promising HI technologies, which enable us to integrate devices made of various materials on various substrates. The FSA employs a stochastic process, where scattered small device blocks are captured by designed places on the host substrate placed in the fluid. The capturing force is, for example, gravity [1], electric force [2] or surface tension [3]. All the recesses can be filled with the devices, if one scatters sufficient number of the blocks.

In this paper, we report on the FSA using low-melting point alloy bumps, which is especially suitable for high performance RTDs.

2. Fluidic Self-Assembly Using Low Melting Point Alloy Bumps

We have already reported the FSA using gravitational force [4]. However, there are several problems to be solved, for example, difficulty in the wiring process and low thermal conductivity between the blocks and the substrates. To overcome these problems we employ the FSA based on low melting point alloys [3, 5]. Figure 1 illustrates their basic process. The host substrate having low-melting point alloy bumps is placed in the fluid, which is heated to keep the bumps melting. A small device block having metal pads is drawn by the surface tension when it contacts the melting bump. Electrical contact as well as mechanical contact can be established simultaneously with this process.

In this study we try to apply this technique to ultra small RTD blocks. A point is that the block consists of only emitter area with thin collector layer as shown in Figure 2. This has significant advantages. First, the excess resistance due to horizontal current path is eliminated with this configuration compared to the conventional planar RTDs, because the current in semiconductor is purely vertical. In addition to this the thermal conductivity is much improved due to the direct contact to the metal via the thin collector layer. These are extremely significant advantages for ultrahigh frequency RTDs having high peak current density. To realize this, we tried to develop the FSA for much smaller (≤10μm) blocks than reported ones (≥30μm) [3].

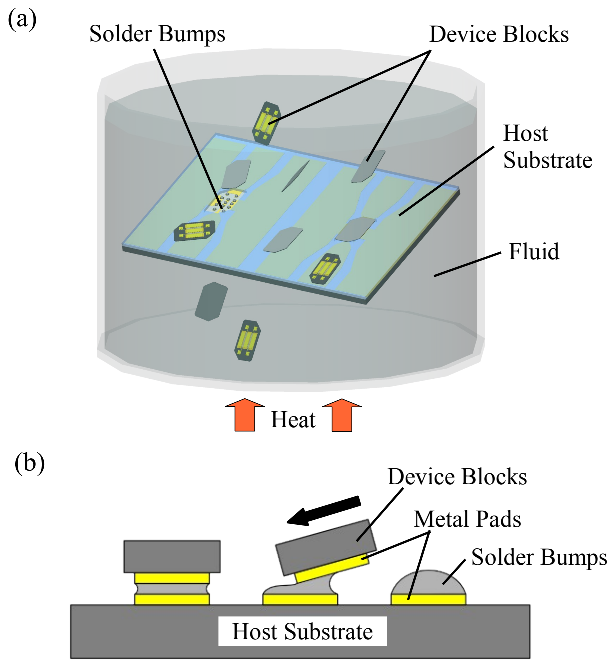

Figure 1. (a) FSA using low-melting point alloy bumps. (b) Self-Assembly by the surface tension.

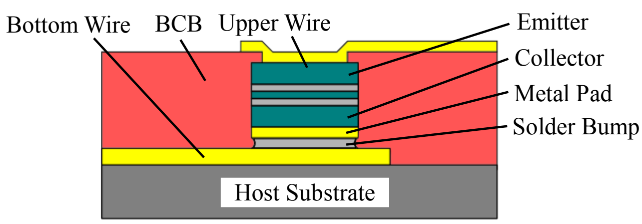

Figure 2. The cross-sectional view of the assembled RTD blocks onto the host substrate.

3. Fabrication of Ultra Small Bumps Using Low-Melting Point Alloy

We first investigated the fabrication process of ultrasmall bump arrays using low-melting point alloys, Bi 44.7%, Pb 22.6%, In 19.1%, Sn 8.3% and Cd 5.3% (melting point, 47°C). Dip-coating method was used, where the host substrate having Au/Cu metal pads is dipped into the molten alloy in acid solution. We found that the form and yield of the bumps are strongly dependent on the alloy temperature and the pH of the solution. By optimizing them we can fabricate ultrasmall bumps having diameter of 2, 4 and 6 μm, which is much smaller than reported ones. The fabricated bumps are shown in Figure 3.

4. Fluidic Self-Assembly Using SiO_2 Test Blocks

We carried out the experiments using test blocks made of SiO_2 to investigate the possibility of the FSA of very small device blocks. The blocks are fabricated as follows. First, 1μm-thick SiO_2 was sputtered on GaAs substrate. Next, Ti/Au was evapolated and lifted-off to form the metal pads. Then, the SiO_2 film was etched by RIE to form circular blocks. The blocks were lifted-off from the substrate by selectively etching the GaAs substrate using a sulfuric-acid-based etchant. The diameter of the fabricated blocks was 12μm.

The FSA was carried out with the experimental setup shown in Figure 4. A piezoelectric vibrator was attached onto the hotplate. The host substrate having low-melting point alloy bumps was placed on it. The SiO_2 blocks kept in diluted HCl (pH 2.0) were supplied on the substrate using a pipette. The diluted HCl was used to remove surface oxide of the bumps, and the vibration makes the blocks mobile on the substrate to stick the bumps. The host substrate temperature was kept at 55°C.

Figure 5 shows the SEM photograph of the assembled block. The block was successfully assembled onto the small bumps. The diameter of the bump was 2μm.

5. Conclusion

Fluidic Self-Assembly using low-melting point alloy bumps was investigated to apply smaller device blocks. FSA of circular blocks having diameter of 12μm was successfully carried out. This is promising for heterogeneous integration of high performance RTDs, because it features low excess resistance and improved thermal performance.

References

[1] H. J. Yeh and J. S. Smith, IEEE Photon. Tech. Lett., Vol.6, No.6, pp706-708, 1994

[2] C. F. Edman, R. B. Swint, C. Gurtner, R. E. Formosa, S. D. Roh, K. E. Lee, P. D. Swanson, D. E. Ackley, J. J. Coleman and M. J. Heller, IEEE Photon. Tech. Lett., Vol.12, No.9, pp1198-1200, 2000

[3] Sean A. Stauth and Babak A. Parviz, PNAS, Vol.103, No.38, pp13922-13927, 2006

[4] Koichi Maezawa, Ikuo Soga, Shigeru Kishimoto, Takashi Mizutani and Kazuhiro Akamatsu, IEICE Trans. Electron., Vol.E91-C, No.7, 2008

[5] Ehsan Saeedi, Shaghayegh Abbasi, Karl F. Böhringer and Babak A. Parviz, FDMP, Vol.2, No.4, pp221-245, 2006

(a)
(b)

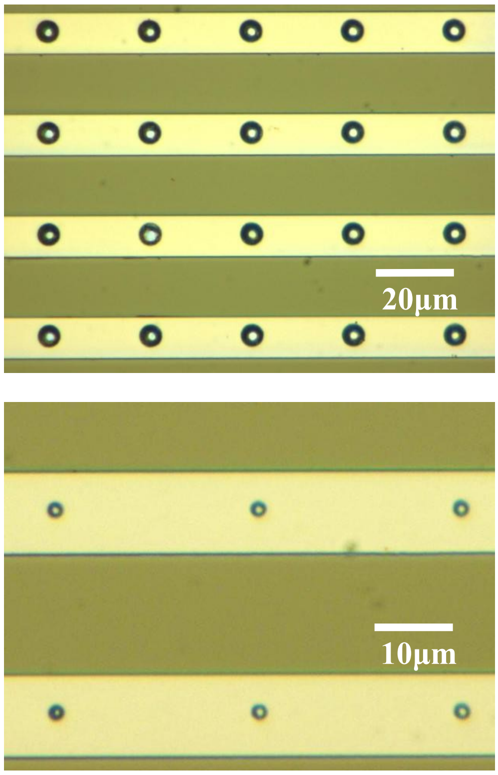

Figure 3. The microphotograph of the low-melting point alloy bumps having diameter of (a) 6μm and (b) 2μm.

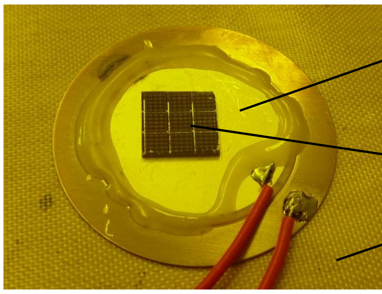

Figure 4. The photograph of the experimental setup.

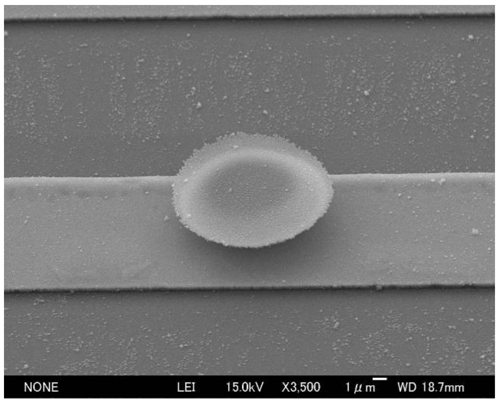

Figure 5. The SEM photograph of the assembled SiO_2 block onto the small bump.