Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp588-589

Operating Principle and Integration of In-Plane Gate Logic Devices

Yuji Komatsuzaki[1,2], Kenichi Saba[1,2], Koji Onomitsu[3], Hiroshi Yamaguchi[3] and Yoshiji Horikoshi[1,2]

[1] School of Science and Engineering, Waseda University
3-4-1 Okubo, Shinjuku-ku, Tokyo 169-8555, Japan
Phone: +81-3-5286-3176 Fax: +81-3-3209-3450 E-mail: y.komatsuzaki@aoni.waseda.jp
[2] Kagami Memorial Laboratory for Materials Science and Technology, Waseda University
2-8-26 Nishiwaseda, Shinjuku-ku, Tokyo 169-0051, Japan
[3] NTT Basic Research Laboratories, NTT Corporation
3-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0198, Japan

1. Introduction

Recently, the size of semiconductor devices has become as small as 50 nm due to advanced micro-fabrication technology. Size reduction has improved device performances considerably. However, this approach is reaching the practical limit caused by the quantum effects and leakage currents. Thus, it is necessary to develop devices based on alternative operation principles.

One concept for a promising semiconductor device is the in-plane gate (IPG) device [1,2]. IPG devices can be operated as logic devices [3], rectifier [4], negative differential resistance device [5] and other functional devices. IPG devices with various functions can be integrated on the same wafer. In contrast to current field-effect transistors used in electronic circuits, the IPG devices have lateral gate structures. Furthermore, the gates are composed of the same semiconductor material as the channels. Therefore, the IPG structure can be fabricated by separating the gate area from the channel.

We investigated logic devices based on an in-plane double gate transistor connected in series with an IPG transistor functioning as variable load resistances. By using the IPG transistor as load resistances high Hi/Low ratio has been achieved, allowing the implementation of reliable logic operations. In this paper, we present the effect of the IPG transistor functioning as load resistances in IPG logic devices. In addition, we demonstrate monolithic IPG NOT-gate devices and it indicates IPG logic devices are suitable for the realization of integrated logic circuits.

2. Experimental Procedure

In-plane gate devices are fabricated on $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ wafers grown by metalorganic vapor phase epitaxy. At the heterostructure interface, a two dimensional electron gas (2DEG) is formed. The 2DEG is located approximately 20 nm below the surface. The 2D electron density and mobility are 3.6×10^{12} cm^{-2} and 6.8×10^{3} $cm^2\cdot V^{-1}\cdot s^{-1}$ at room temperature, respectively.

After a proper surface treatment, the wafer is spin coated with resist (ZEP520A). The device patterns are written on the wafer surface by electron beam lithography. The insulating trenches are formed by electron cyclotron resonance reactive ion etching (ECR-RIE). Trenches as narrow as 40 nm are realized by the optimized process. The etch depth is approximately 30 nm and reaches deeper than the location of the 2DEG. Thus, the gates and the channels are separated by the trenches. All measurements are performed in the dark.

3. Results and Discussion

Operating Principle of IPG Logic Devices

The logic circuit of an in-plane double gate transistor (IPDGT) connected in series with another IPDGT working as a variable resistance is shown in Fig.1. The input device is named IPDGT1, and the load device is named IPDGT2. The input signals V_{In1} and V_{In2} are applied to the left and right gate of IPDGT1, respectively. The output voltage V_{Out} is applied to the gates of IPDGT2. The channel width and length of the IPDGTs are 90 nm and 600 nm, respectively. The bias voltage, the Hi-signal and the Low-signal are 1.0V and 0.0V, respectively. This IPG logic device operates as a NOR-gate as demonstrated in Fig. 2(a). The operation of the logic device is explained as follows. When a Hi-signal is applied to each gate of the IPDGT1, its channel opens and V_{Out} shifts to low voltage. After that, V_{Out} is applied to the gates of IPDGT2 and its channel closes. As a result, V_{Out} is close to 0.0V. When a Low-signal is applied to each gate of the IPDGT1, V_{Out} becomes close to 1.0V.

When the gate voltage of IPDGT2 is clamped to either 0.0V or 1.0V, the input-output characteristics and the current through the channel of IPDGTs are shown in Fig. 2(b). The logic device does not show high Hi/Low ratio outputs anymore and the power consumption becomes high. The power consumption of the logic device using an IPDGT as

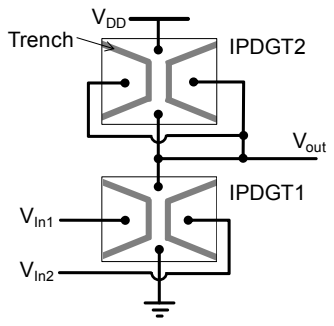

Fig. 1 Logic circuit diagram of IPDGT1 connected in series with IPDGT2 working as a variable resistance.

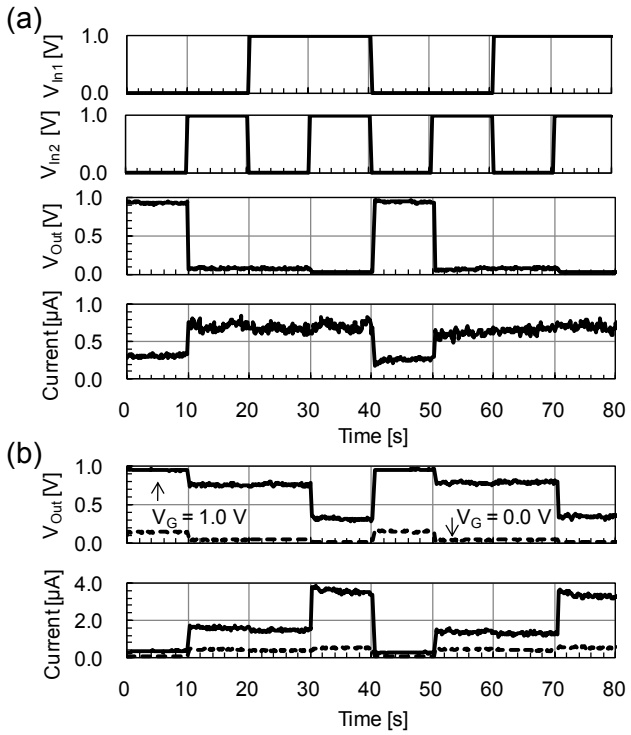

Fig. 2 (a) Input-output characteristics and current through the channel of the IPG logic device shown in Fig. 1. (b) Input-output characteristics and current through the channel of the IPG logic device. The solid line shows the characteristic when gates voltage of IPDGT2 is 1.0 V. The dotted line shows the characteristic when gates voltage of IPDGT2 is 0.0 V.

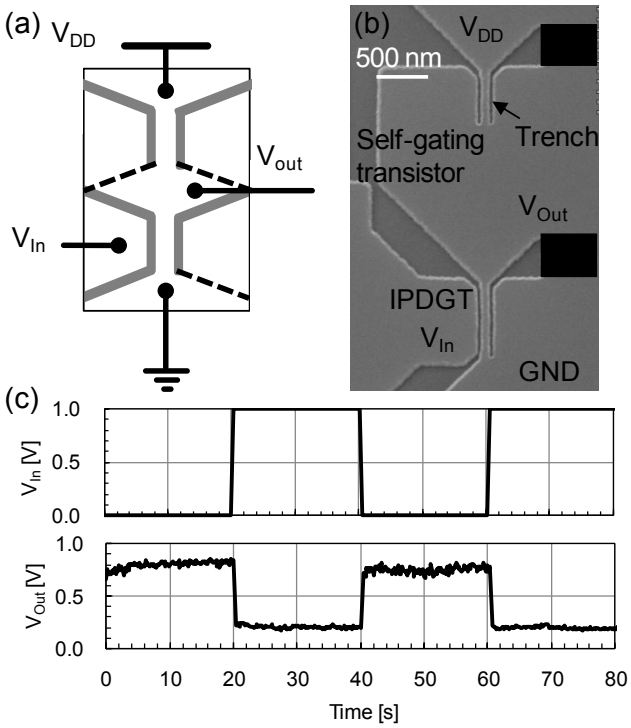

Fig. 3 (a) Logic circuit diagram of IPG NOT-gate device. The dotted lines are the removed trenches. (b) SEM image of the IPG NOT-gate device. (c) Input-output characteristics of the IPG NOT-gate device.

a variable resistance is greatly decreased in comparison to a logic device functioning with a fixed resistance.

IPG NOT-gate devices

The logic device presented in the previous section is short-circuited the source and the gate terminal of IPDGT2 which have been separated by a trench. Therefore, by removing the trench separating source and gate of IPDGT2 the logic device geometry is simplified, while allowing the logic device operations. In addition, the wiring between two transistors can be removed. A NOT-gate is fabricated when one input-gate of NOR device is fixed to 0 V (GND). Figure 3(a) shows the NOT-gate circuit of an IPDGT connected in series with in-plane self-gating transistor working as a variable resistance. The bias voltage, the Hi-signal and the Low-signal are 1.0V and 0.0V, respectively. The input-output characteristic of the monolithic IPG NOT-gate device is shown in Fig. 3(c). The Hi/Low ratio is high enough for reliable logic operations. In addition, this result is demonstrated that IPG logic devices are fabricated by forming trenches without wiring. It is because the source, drain and gate are in the same plane of the devices and it indicates IPG logic devices can be easily integrated with less wiring.

4. Conclusions

In-plane gate logic devices have been fabricated by using InGaAs/InAlAs 2DEG wafers. Logic devices are formed by an in-plane double gate transistor connected in series with an IPG transistor functioning as variable resistances. By using the IPG transistor as variable resistances high Hi/Low ratios have been achieved, allowing the implementation of reliable logic operations. Furthermore, the logic devices operate at low current in comparison to logic devices under a clamped gate voltage at the load device. In addition, because the source, drain and gate are located in the same plane, it is possible to fabricate the IPG logic devices by forming trenches without wiring. This leads to a considerable reduction of the number of terminals and wiring for the integrating of logic circuits.

Acknowledgements

This work is partly supported by the Global COE Program "Practical Chemical Wisdom" from the Ministry of Education, Culture, Sports, Science and Technology (MEXT).

References

[1] A. D. Wieck and K. Ploog, Appl. Phys. Lett. **56** (1990) 928.

[2] T. Müller, A. Lorke, Q. T. Do, F. J. Tegude, D. Schuh, and W. Wegscheider, Solid-State Electron. **49** (2005) 1990.

[3] S. Reitzenstein, L. Worschech, C. R. Müller, and A. Forchel, IEEE Electron Device Lett. **26** (2005) 142.

[4] A.M. Song, M. Missous, P. Omling, A.R. Peaker, L. Samuelson, and W. Seifert, Appl. Phys. Lett. **83** (2003) 1881.

[5] Y. Komatsuzaki, K. Higashi, T. Kyougoku, K. Onomitsu and Y. Horikoshi, Jpn. J. Appl. Phys. **49** (2010) 104001.