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The Influence of a SnInGaZnO Electron Barrier Layer on the performance of Low-Driving Voltage InGaZnO Thin-Film Transistors

Hau-Yuan Huang[1], Shui-Jinn Wang[1,2], Chien-Hung Wu[3], Chen-Kuo Chiang[1], Yen-Chieh Huang[1], and Je-Yi Su[1]

[1] Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan.
[2] Advanced Optoelectronic Technology Center, National Cheng Kung University, Taiwan
[3] Department of Electronics Engineering, Chung Hua University, Hsinchu, Taiwan.
Phone: +886-6-2763882 E-mail: sjwang@mail.ncku.edu.tw

1. Introduction

In the nowadays liquid crystal display (LCD) industries, the power consuming rate has come into public notice as an important issue. Different techniques have given rise to the revolution of LCDs, such as LED backlights and high carrier mobility transparent oxide semiconductor materials (TOS). In the aspect of thin-film-transistors (TFTs) engineering, indium gallium zinc oxide (InGaZnO) has been demonstrated as one of the promised candidate for channel material over others [1]. However, the problems as inappropriate threshold voltages and negative turn-off voltages (V_{off}) is yet needed to be overcome in practical application to reduce power consumption during stand-by [2][3]. In addition, the high device operating voltage causes superfluous energy loss. In this study, high-k metal gate is employed to decrease the operating voltage of TFTs. Tin-doped InGaZnO layer (SnInGaZnO) fabricated by RF co-sputtering was proposed to add in between source/drain (S/D) region and InGaZnO channel to adjust V_{th} and V_{off} of InGaZnO-TFTs simultaneously. Experimental results reveal that both V_{th} and V_{off} can be tuned toward positive values, also, I_{on}/I_{min} is increased, and substhreshold swing is reduced at the same time.

2. Experiments

Fig. 1 depicts schematically the device structure of the proposed bottom gate InGaZnO-TFTs with additional SnInGaZnO-EBL. TaN was employed as the gate electrode, 50-nm-thick HfSiO was used as gate insulator, 25-nm-thick RF sputtered InGaZnO as channel layer, The co-sputtering condition of P_{SnO} = 40 W and $P_{InGaZnO}$ = 80 W was employed to fabricate the SnInGaZnO EBL, and aluminum was utilized as S/D electrodes. Note that there is no need for extra mask since EBL was deposited utilizing the same mask of S/D electrodes, hence reduces the process complexity.

3. Results and Discussion

Fig. 2 shows carrier density and Hall mobility of the SnInGaZnO films obtained by Hall measurement. Fig. 3 shows the O1s core level spectra of SnInGaZnO films obtained by x-ray photoelectron spectroscopy (XPS). An evident transition of Sn bonding type from SnO (529.7 eV) into SnO_2 (529.9 eV) are observed as $P_{SnO} > 40$ W [4], indicating that the appearance of SnO_2 would decrease the carrier density as the downward line shown in Fig. 2. Fig. 4 exhibits the band-gap values of SnInGaZnO and InGaZnO obtained from optical absorption measurement [5]. The derived band-gap is 3.62 eV for InGaZnO and 3.38 eV for SnInGaZnO, indicating tin doping in InGaZnO leads to a band-gap narrowing of about 0.24 eV.

Fig. 5 shows I_D-V_G characteristics of the proposed InGaZnO-TFTs with low-driving voltage (≤ 2 V). Note that the transfer curves shift toward positive V_G-axis as t_{EBL} was increased, which should be due to the high SnInGaZnO barriers in source/SnInGaZnO/InGaZnO/SnInGaZnO/drain route, an additional gate bias is needed to lower the induced barriers, and the barrier is high for thick SnInGaZnO since the same drain bias is divided up by an extended source-drain distance with same InGaZnO length. It is interesting to see that V_{off} can be tuned to 0 V @ t_{EBL} = 250 nm, and I_{min} can be reduced from 4.6×10^{-10} A @ t_{EBL} = 0 nm to 2.7×10^{-11} A @ t_{EBL} = 250 nm. As t_{EBL} = 500 nm, V_{off} keeps shifting to 0.2 V. It is ascribed to the fact that the SnInGaZnO layer provides an additional barrier height to block channel electrons from source/drain electrodes. Essentially, a thick SnInGaZnO would induce a high series resistance and in turn causes a large voltage drop across the S/D and channel interface, as the results, I_{min} would slightly raises, and I_{on} is decreased. Fig. 6 shows $\sqrt{I_D}$-V_G characteristics to calculate the saturation mobility, the carrier mobility decayed from 14.53 cm^2/V-s to 10.29 cm^2/V-s with thickened SnInGaZnO. Therefore, with appropriate SnInGaZnO thickness applied to the InGaZnO-TFTs, electrical performance can be optimized, and the extracted device parameters are shown in Table 1 with the best condition of I_{on}/I_{off}, S.S, V_T, V_{off}, and mobility are 1.9×10^6, 0.077 V/dec, 0.55 V, 0 V and 13.39 cm^2/V-s, respectively @ t_{EBL} = 250 nm (note that I_{off} is defined at V_G = 0 V).

4. Conclusions

We have investigated the basic characteristics of alloyed-SnInGaZnO films and its influence on the electric performance of a-InGaZnO-TFTs. Through the use of a SnInGaZnO electron barrier layer, better switch property of $I_{on}/I_{off} = 1.9\times10^6$, better gate control ability of S.S = 0.077 V/dec, appropriate turn-off voltage of V_{off} = 0 V, and high mobility of μ_{sat} = 13.39 cm^2/V-s have been obtained. The engineering of source/drain barrier layer proposed in this work is expected to improve the performance of conventional a-InGaZnO devices in future applications.

Acknowledgements

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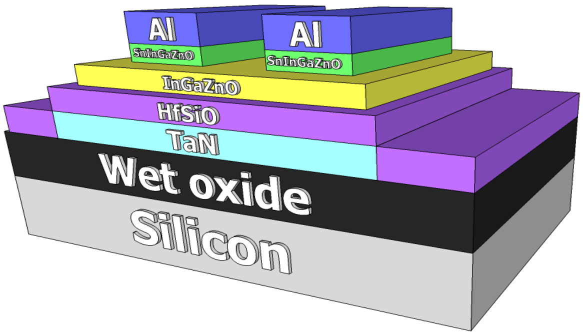

Fig. 1 Schematic device structure of the proposed InGaZnO-TFT with SnInGaZnO layer.

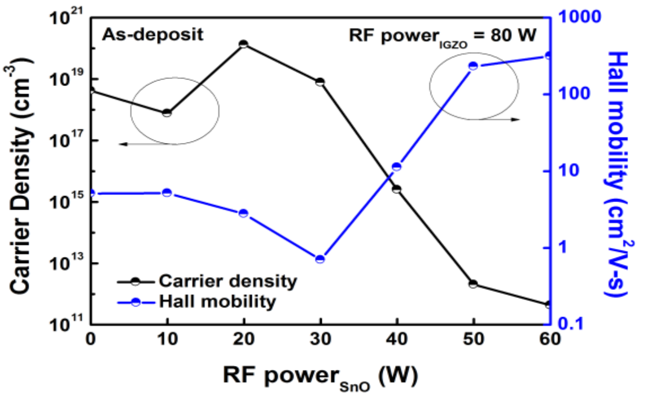

Fig. 2 Carrier density and Hall mobility of SnInGaZnO film with different SnO sputtering power obtained by Hall measurement.

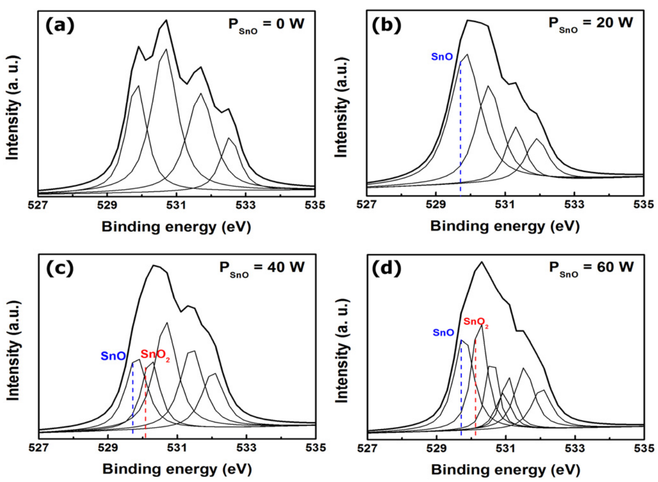

Fig. 3 Evolution of O 1s core level spectra of SnInGaZnO films as a function of SnO sputtering power. (a) P_{SnO} = 0 W. (b) P_{SnO} = 20 W. (c) P_{SnO} = 40 W. (d) P_{SnO} = 60 W. The colored lines in each figure indicate the SnO and SnO_2 peaks.

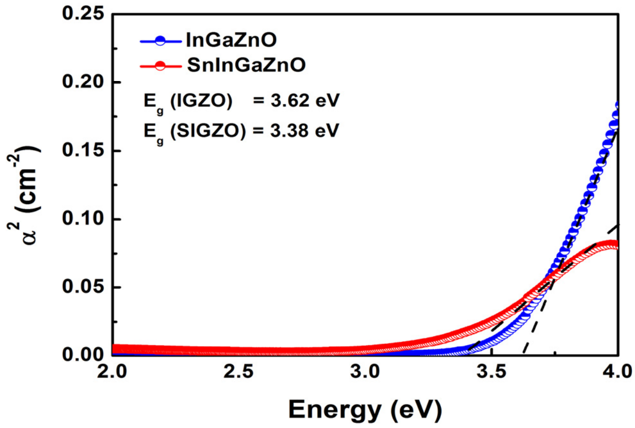

Fig. 4 Absorption characteristics of the sputtering deposited InGaZnO and SnInGaZnO films.

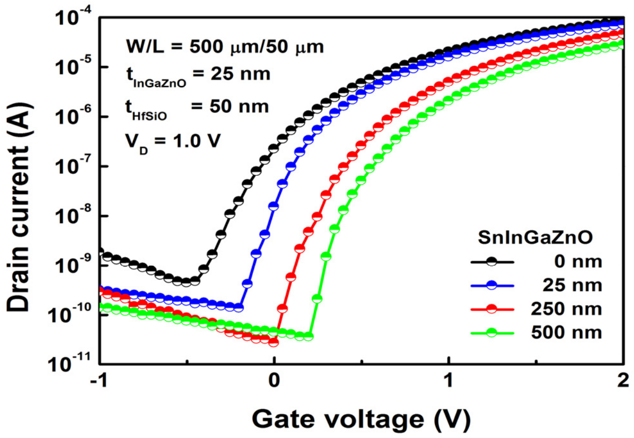

Fig. 5 I_{DS}-V_{GS} characteristics of the low-driving voltage InGaZnO-TFTs with different SnInGaZnO-EBL thicknesses.

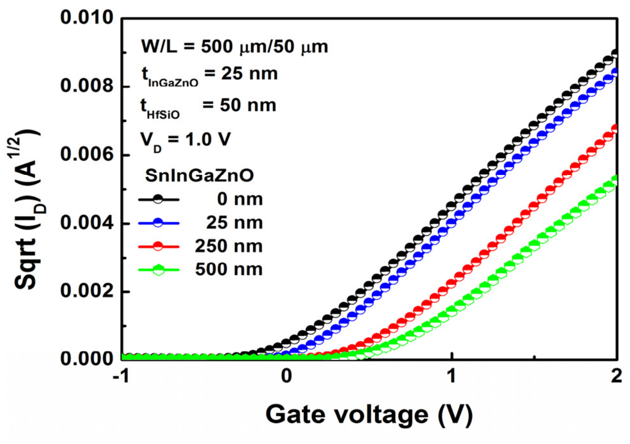

Fig. 6 $\sqrt{I_{DS}}$-V_{GS} characteristics of the low-driving voltage InGaZnO-TFTs with different SnInGaZnO-EBL thicknesses.

TABLE I The extracted device parameters of InGaZnO-TFTs with different SnInGaZnO thicknesses

SIGZO (nm)	I_{on}/I_{off}	S.S (V/dec)	V_T (V)	V_{off} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	I_{on} (A)
0	3.6×10^2	0.13	0.06	-0.45	14.53	8.1×10^{-5}
25	4.6×10^3	0.092	0.16	-0.20	14.53	7.1×10^{-5}
250	1.9×10^6	0.077	0.55	0	13.39	4.6×10^{-5}
500	8.5×10^5	0.070	0.64	0.20	10.25	2.8×10^{-5}