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High-Voltage SiC Power Devices for Energy Electronics

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1. Introduction

High-efficiency electric power conversion is an essential technology for energy saving. The efficiency of power converters/inverters strongly relies on the performance of power semiconductor devices employed in the power electronic systems. Silicon carbide (SiC) is a newly-emerging wide bandgap semiconductor, by which high-voltage, low-loss power devices can be realized owing to its superior properties [1-3]. Fig. 1 shows the major territories of individual unipolar and bipolar power devices for Si and SiC in terms of the rated blocking voltage [3]. It is expected that SiC unipolar devices will replace Si unipolar/bipolar devices in the blocking-voltage range from 300 V to about 4500 V. For ultrahigh-voltage applications above 4500 V, SiC bipolar devices will be attractive. This paper reviews recent progress in high-voltage SiC power devices. In particular, ultrahigh-voltage PiN diodes and high-current gain BJTs obtained in the authors' group are presented.

2. Improvement of material quality

The density of dislocations in SiC wafers and epilayers has been remarkably reduced in the last several years. The wafer size and uniformity of epilayers are also being improved. The quality of state-of-art SiC epi-wafers is sufficient for fabrication of unipolar devices, and the volume production of 600-1200 V SiC SBDs and MOSFETs has started. In the next step, SiC bipolar devices are of academic and technological interest, where dynamics of carrier recombination should be understood and controlled.

The authors succeeded in elimination of the carrier-lifetime killer in SiC by thermal treatment. The lifetime killer has been identified as the $Z_{1/2}$ center, which is located at $E_C - 0.65$ eV [4]. Fig. 2 depicts the DLTS spectra taken from an n-type 4H-SiC epilayer before and after thermal oxidation at 1300°C for 5 h. The $Z_{1/2}$ and $EH_{6/7}$ ($E_C - 1.55$ eV) centers are dominant with a trap concentration of (2-5)x10^{12} cm^{-3} in the as-grown epilayer, but both the DLTS peaks disappeared (< 1x10^{11} cm^{-3}) after the oxidation [5]. The authors suggest that C interstitials emitted from the SiO_2/SiC interface may diffuse into the bulk region of the epilayer during oxidation, and recombine with C vacancies (likely related to the $Z_{1/2}$ center), leading to elimination of the $Z_{1/2}$ center. Fig.3 shows the μ-PCD decay curves at room temperature obtained from a 122 μm-thick epilayer before (as-grown) and after thermal oxidation. The measured lifetime was improved from 0.68 μs to 6.6 μs after thermal oxidation. The carrier lifetime can be further enhanced to 13 μs by passivating the surface with deposited oxides annealed in NO [6]. The authors found clear correlation between the effects of surface passivation and the density of interface states at SiO_2/SiC MOS structures.

3. Ultrahigh-voltage SiC PiN diodes

Alleviation of electric field crowding in ultrahigh-voltage (> 10 kV) devices is a challenge. The authors have proposed a novel junction termination structure, space-modulated JTE [7]. In this structure, the multiple rings are formed at the outer edge of each RESURF-type JTE. The width and spacing of individual rings are modulated so that the effective JTE dose is gradually decreasing toward the outer edge. The major benefits of this JTE structure include the wide optimum window (range) in the JTE dose to attain nearly ideal blocking voltage.

Fig.4 demonstrates the current density – voltage characteristics of a mesa SiC PiN diode with a space-modulated JTE structure (total length of JTE: 600 μm) [8]. The thickness and doping concentration of the lightly-doped n-type epilayer were 147 μm and 6.4x10^{14} cm^{-3}, respectively, by which the ideal blocking voltage can be estimated as 16.1 kV [9]. The fabricated PiN diodes exhibited non-destructive breakdown at 15.4 kV, which reaches 95% of the ideal value. The breakdown voltage increased with elevating the device temperature.

4. High-current-gain SiC BJTs

SiC BJTs have suffered from relatively low current gains (30-70), due to short carrier lifetimes and poor surface passivation. Since the authors succeeded in solving these problems as described above, an original fabrication process has been developed. The fabricated BJTs are of a double-mesa structure with all epitaxial junctions. The thickness and doping concentration are 1.2 μm and 2x10^{19} cm^{-3} for the emitter, 0.35 μm and 2x10^{17}-1x10^{18} cm^{-3} for the base, and 10 μm and 1x10^{16} cm^{-3} for the collector. The defect reduction process (thermal oxidation) and the improved surface passivation were employed in the device fabrication. Continuous growth of the emitter junction is another key factor to obtain high current gains.

The Gummel plot of SiC BJT fabricated on (000-1) with 20-μm-wide finger and {1-100} sidewalls is shown in Fig.5. The ideality factor of the collector current is 1.0, and a record current gain of 335 was achieved in this BJT [10]. On the (0001) face, a fabricated BJT also exhibited a high current gain of 257. These values are twice as large as the

previous record gain [11].

5. Conclusions

Recent progress in SiC power devices has been reviewed. The carrier-lifetime-killing defect in SiC has been almost eliminated by thermal oxidation, and the surface recombination has significantly been reduced by passivation with nitrided oxides. SiC PiN diodes with an original junction termination structure exhibited a nearly ideal blocking voltage of 15 kV. Combining several techniques, high current gains (> 250) have been achieved in SiC BJTs.

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References

[1] M. Bhatnager and B.J. Baliga, IEEE Trans. Electron Devices, **40** (1993) 645.
[2] H. Okumura, Jpn. J. Appl. Phys., **45** (2006) 7565.
[3] T. Kimoto, *Technical Digests of 2010 Symp. on VLSI Technology* (Honolulu, 2010), p.9.
[4] K. Danno, D. Nakamura, and T. Kimoto, Appl. Phys. Lett., **90** (2007) 202109.
[5] T. Hiyoshi and T. Kimoto, Appl. Phys. Express, **2** (2009) 041101.
[6] T. Kimoto, Y. Nanen, T. Hayashi, and J. Suda, Appl. Phys. Express, **3** (2010) 121201.
[7] G. Feng, J. Suda, and T. Kimoto, *presented at Spring Meeting of Japan Society of Applied Physics* (2011), 25p-BL-17.
[8] H. Niwa, G. Feng, J. Suda, and T. Kimoto, *presented at ICSCRM2011* (Cleveland, 2011).
[9] A.O. Konstantinov, Q.Wahab, N. Nordell, and U. Lindefelt, Appl. Phys. Lett., **71** (1997) 90.
[10] H. Miyake, T. Kimoto, and J. Suda, IEEE Electron Device Lett., **32** (2011) 841.
[11] K. Nonaka et al.,Phys. Stat. Sol. (a), **206** (2009) 2457.

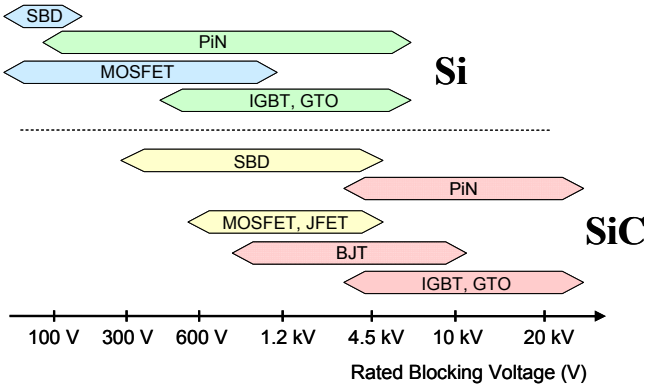

Fig. 1 Major territories of individual unipolar and bipolar power devices for Si and SiC in terms of the rated blocking voltage.

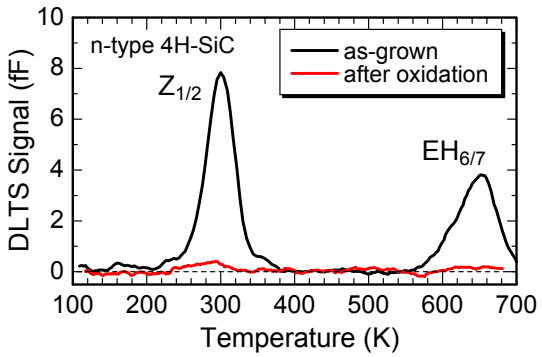

Fig.2 DLTS spectra taken from an n-type SiC epilayer before and after thermal oxidation at 1300°C for 5 h.

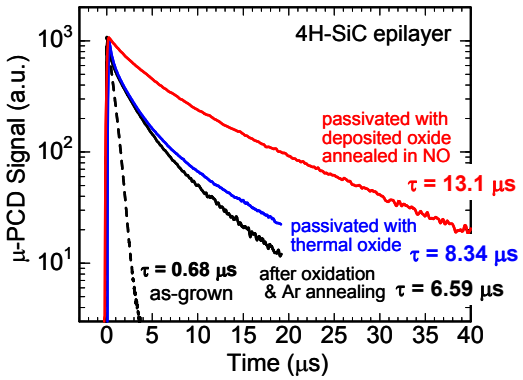

Fig.3 μ-PCD decay curves at room temperature obtained from a 122 μm-thick SiC epilayer before (as-grown) and after thermal oxidation.

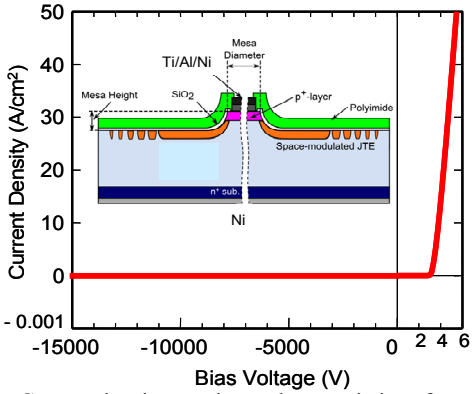

Fig.4 Current density – voltage characteristics of a mesa SiC PiN diode with a space-modulated JTE structure.

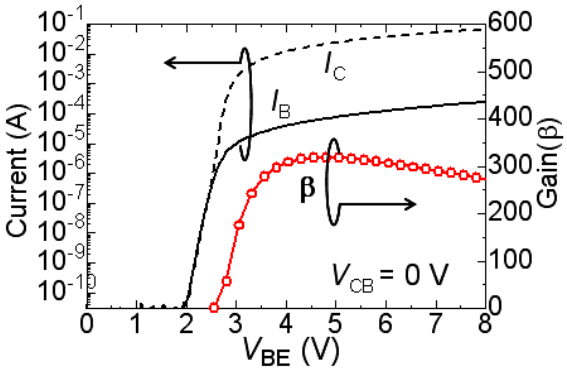

Fig.5 Gummel plot of SiC BJT fabricated on (000-1) with 20-μm-wide finger and {1-100} sidewalls.