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Thermodynamic Control of Interface Layer Formation in High-k Gate Stacks on 4H-SiC

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1. Introduction

SiC has been long investigated for the power device applications [1]. SiC crystalline properties have been considerably improved, but excellent gate stacks have still not been successfully achieved. The big issue is how to improve the interface on SiC. In addition, high-k dielectrics will provide a wide range of freedom to make SiC devices more versatile.

This paper discusses both interface layer formation on SiC and high-k implementation in SiC gate stacks on the basis of thermodynamic consideration. In addition the difference between Si- and C-faces of 4H-SiC is discussed in terms of gate stack characteristics.

2. Thermodynamic Consideration of SiC system

It is known that the oxidation of SiC occurs at SiC/SiO_2 interface as that of Si [2]. The differences are that (i) CO is accompanied with the oxidation of SiC, and (ii) higher temperature (>1000ºC) is needed to oxidize SiC. The C introduction into oxidized SiO_2 will lead to significantly poor quality of SiO_2. Therefore, the lower temperature oxidation would be beneficial for both process optimization and SiO_2 quality improvement. Deposited insulators, however, generally show poor qualities of both interface and bulk properties.

To overcome those challenges, we have prepared the Si/SiC stack structure for the starting substrate. There are two important points. SiO_2 is thermally grown and the SiC oxidation can be minimized as slight as possible by employing a low temperature oxidation, because the oxidation temperature is quite different between SiC and Si. This fact comes from the thermodynamic difference between them. The technique of oxidizing the deposited Si on SiC was already reported [3], in which thick Si was used. In that case, it was needed to oxidize Si at relatively higher temperature (>1000ºC) and might degrade the interface. Therefore, nm-thick Si on SiC should be favorable for achieving good interface on SiC.

Table 1 shows the process flow of n-type (N-doped) 4H-SiC (Si- and C-faces) MOS capacitors. Backside ohmic contact was achieved by Ni-silicide formation at 900ºC.

3. Results and Discussion

Fig. 1 shows the schematic cross section of the gate stack formation process. **Fig. 2** shows a XTEM image of $HfO_2/SiO_2/SiC$(Si-face) gate stack. A good SiC/SiO_2 interface is observed. **Fig. 3** shows SiO_2 thickness grown on SiC with Si- and C-face as a function of oxidation time at 800ºC. C-face SiC shows much faster oxidation than Si-face one [4]. The results indicate that much more C should be contained in SiO_2 on C-face SiC, while the oxidation at 800ºC seems to saturate with the time for Si-face SiC after the oxidation of deposited Si. Therefore, the interface should be quite good, because only a very small amount of C was introduced into the interfacial SiO_2 layer on Si-face sample. **Fig. 4** compares C-V characteristics between (a) Si-face and (b) C-face SiC gate stacks as a parameter of measurement frequency, where the oxidation was performed at 800ºC for 50 min. CET of the gate dielectric film was ~10 nm. It is clearly seen that Si-face SiC shows a definitely better C-V with a reasonable V_{FB}. C-V characteristics in SiC MIS capacitor without Si deposition was severely degraded with huge leakage current because of very low oxidation rate at 800ºC (data not shown).

Finally we studied the photo C-V characteristics to detect interface states effects on SiC, because it was hard to see the deep interface states in SiC capacitors in the dark at room temperature. **Fig. 5** shows the C-V characteristics under the fluorescent lamp. It seems that only a small shift in C-V is observed even at 100 Hz, though the light might affect only an edge region.

A considerable benefit of thin Si deposition on SiC before the oxidation is that it is easy to form thermally grown SiO_2 on SiC at a relatively low temperature without oxidizing SiC. In addition high-k deposition followed by PDA can be also utilized. This is quite a different concept from the past research [3].

4. Conclusions

We have demonstrated quite good C-V characteristics in $HfO_2/SiO_2/SiC$ MOS gate stacks by oxidizing Si/SiC (Si-face) at 800ºC, in which very thin Si layer was deposited in advance on SiC surface. We would like to mention that thermodynamic control of the interface on SiC should be quite robust and tough against the device operation and manufacturing process. Furthermore, high-k dielectric film has been successfully introduced to SiC gate stack. There is obviously a room for further optimizing the thickness and/or processing temperature, but the present method will be a very promising technique for achieving stabilized SiC gate stacks.

References

[1] J. A. Cooper, Jr. and A. Agarwal, Proc. IEEE **90** (2002) 956.

[2] J. A. Costell and R. E. Tressler, J. Am. Ceram. Soc. **64** (1981) 327.

[3] J. Tan et al., Appl. Phys. Lett. **70** (1977) 2280.

[4] Y. Song et al., J. Appl. Phys. **95** (2004) 4953.

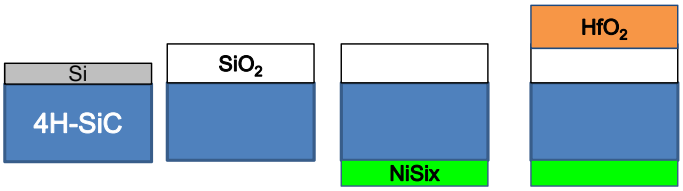

Fig. 1. Schematics of gate stack formation process in $HfO_2/SiO_2/SiC/NiSix$.

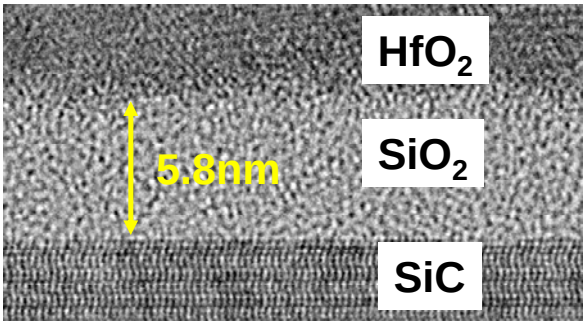

Fig. 2. XTEM image of $HfO_2/SiO_2/SiC$(Si-face). SiC/SiO_2 interface is quite flat.

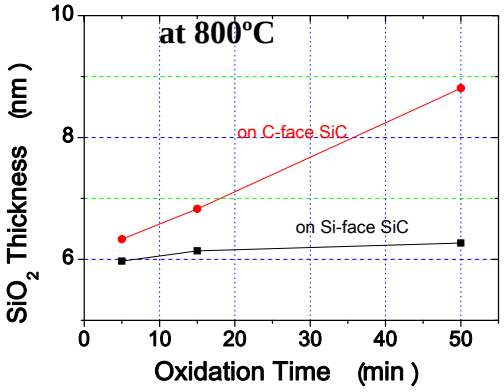

Fig. 3. SiO_2 thickness as a function of oxidation time for deposited Si on both Si- and C-face SiC at 800°C. Note that C-face SiC is also considerably oxidized after the oxidation of deposited Si.

Table 1 Process flow of SiC MOS capacitors

Si- and C-face 4H-SiC
RCA cleaning
Si deposition (~3 nm) / EB evaporation
Thermal oxidation at 800°C
Back metallization / Ni evaporation
PMA / N_2 940°C, 5 min
FGA / 400°C 30 min
HfO_2 deposition / rf-sputtering (~10 nm)
PDA / 0.1% O_2, 500°C 30 sec.
Au electrode evaporation

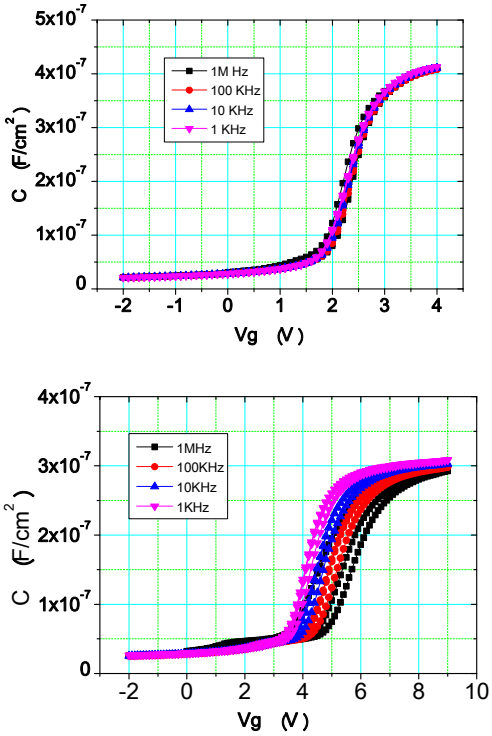

Fig. 4. (*upper*) Bi-directional C-V characteristics in $HfO_2/SiO_2/SiC$ (Si-face) as a parameter of measurement frequency. Only a very small hysteresis is observed. (*lower*) $HfO_2/SiO_2/SiC$ (C-face). Large frequency dispersion and hysteresis are observed. Both SiO_2 was grown at 800°C.

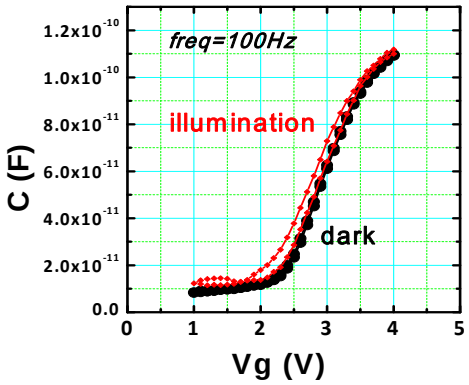

Fig. 5. C-V characteristics in $Au/HfO_2/SiO_2/SiC$ (Si-face) at 100Hz in dark and under illumination. Not so significant degradation is observed even at 100Hz.