

Characteristics of 4H-SiC p-Channel MOSFETs with Ion-Implanted Buried Channel

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1. Introduction

A number of discrete low-loss and high-power SiC Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) have been demonstrated to date. It is another advantage that those SiC devices operate at high temperature such as 300°C. Si-based system drive circuitry, however, cannot work at such high temperatures, thus thermal isolation schemes are needed to protect the Si-based drive circuitry. On the other hand, SiC integrated circuits (ICs) composed of SiC power MOSFETs and SiC Complementary MOS (CMOS) circuits do not require such thermal isolation schemes. These merits improve the power density of SiC power modules, cost reduction and reliability drastically.

SiC CMOS devices are composed of n- and p-channel MOSFETs, but SiC p-channel MOSFETs have not been developed so far. The poor channel property of SiC p-channel MOSFETs is one of the serious problems. We have reported that wet oxidation could provide relatively high channel mobility (15.6 cm²/Vs) and low threshold voltage for Si-face 4H-SiC(0001) p-channel MOSFETs [1]. Furthermore, we fabricated Si-face 4H-SiC(0001) CMOS devices utilizing the wet gate oxidation processing [2]. For further development of SiC CMOS technology, it is desirable that the channel properties of both n- and p-channel MOSFETs, such as channel mobility and threshold voltage, can be controlled. Additional doping to the channel region, so called “buried channel” structure, is effective method to control the channel properties. There are, however, few reports on SiC p-channel MOSFETs with buried channel structure. In this study, we investigated the effects of buried channel on electrical properties of 4H-SiC n- and p-channel MOSFETs.

2. Device Fabrications

We fabricated 4H-SiC n- and p-channel MOSFETs on 8° off-axis 4H-SiC Si-face p- and n-type epi-wafers (N_a - N_d and N_d - N_a = 5×10^{15} /cm³), respectively. The source/drain regions of n- and p-channel MOSFETs were formed by ion implantation with box profile of P⁺ and Al⁺ with the concentration of 2×10^{20} /cm³ to the depth of 0.3 μm, respectively. The buried channel structures for n- and p-channel MOSFETs were formed by ion implantation of N⁺ and Al⁺ with box profile with several concentrations to the depth of 0.2 μm, respectively. Simulated final doping profile under the gate is shown in Fig. 1. The thermal gate oxidation was

performed in wet O₂ ambient at 1200°C. Following the gate oxidation, in-situ annealing in Ar was carried out at 1200°C for 30 min. The thickness of the gate oxide was 45±1 nm. The gate electrode was phosphorus doped n-type poly-Si. The designed channel length and width were 100 and 150 μm, respectively.

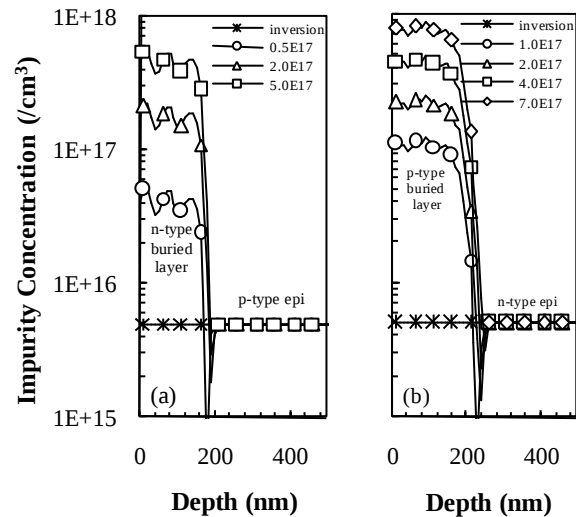


Fig. 1 Simulated final doping profile under the gate for (a) n- and (b) p-channel MOSFETs.

3. Results and discussion

4H-SiC n-channel MOSFETs with buried channel

Figure 2 shows the field effect channel mobility of 4H-SiC n-channel MOSFETs with and without buried channel as a function of the gate voltage (V_g). The concentrations of nitrogen ions implanted into buried channel layer ($N_{bc,N}$) are 0.5×10^{17} to 5.0×10^{17} /cm³ at the depth of 0.2 μm, as shown in Fig. 1 (a). The channel mobility of the inversion-type n-channel MOSFET (without buried layer) is very low (~ 1 cm²/Vs). This is due to large density of the interface states near the conduction-band for the wet oxidized 4H-SiC MOS structure. The channel mobility of samples with buried channels increases and the threshold voltage decreases with increasing the $N_{bc,N}$. The n-channel MOSFET with buried channel at the $N_{bc,N}$ of 5.0×10^{17} /cm³ indicates “normally-on” characteristics in depletion mode. The n-channel MOSFET with buried channel at the $N_{bc,N}$ of 2.0×10^{17} /cm³ operates in partial enhancement/depletion

mode with “normally-off” characteristics. In enhancement/depletion mode, carrier conduction through the buried channel layer away from the SiO₂/SiC interface occurs at the low V_g. This conduction does not suffer from the surface scattering, and thus the channel mobility increases approaching to the bulk mobility. When the high V_g is applied, electrons are accumulated beneath the SiO₂/SiC interface, and the carrier conduction is affected by the interface states. This is the reason for the decrease of channel mobility of buried-channel MOSFETs at high V_g.

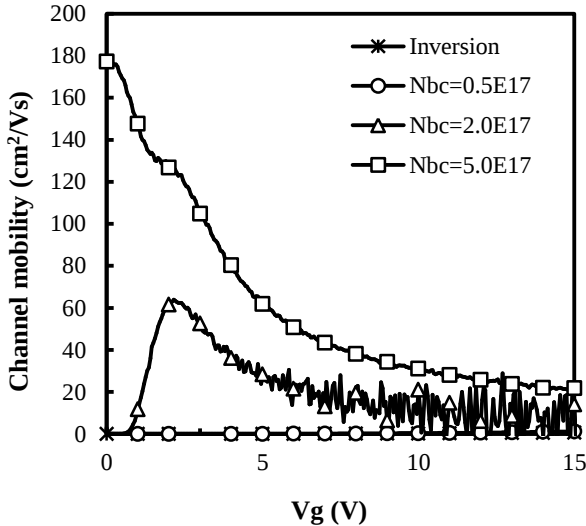


Fig. 2. Channel mobility of 4H-SiC n-channel MOSFETs with/without buried channel as a function of V_g.

4H-SiC p-channel MOSFETs with buried channel

Figure 3 shows the field effect channel mobility of 4H-SiC p-channel MOSFETs with and without buried channel as a function of the V_g. The concentrations of aluminum ions implanted into buried channel layer (N_{bc,Al}) are 1.0×10^{17} to 7.0×10^{17} /cm³ at the depth of 0.2μm, as shown in Fig. 1 (b). Inversion-type p-channel MOSFET indicates higher channel mobility (15cm²/Vs) than inversion-type n-channel MOSFET (~1cm²/Vs). This may be due to the lower density of interface states near the valence-band in comparison with that of near the conduction-band. The effects of buried channel layer on p-channel MOSFETs are quite different from those on n-channel MOSFETs. The channel mobility of p-channel MOSFETs does not increase using buried channel structure even though the N_{bc,Al} are so high that “normally-on” characteristics is observed. As noticed above, it is expected that buried-channel MOSFETs have carrier conduction through the buried channel layer away from SiO₂/SiC interface and thus indicate higher channel mobility than inversion-type MOSFETs. In the case of SiC p-channel MOSFETs, it is considered that the channel mobility does not increase because of the low carrier density at the implanted buried channel layer due to the large ionization energy of acceptors and/or low mobility of the implanted buried channel layer. It is noticeable that “normally-on” samples in Fig. 3 have small hump around the V_g of -3V. This hump may be originated from the con-

duction through the buried channel. In the case of n-channel MOSFETs, this hump might become very large and predominant, as shown in Fig. 3. Increase in the threshold voltage with an increase in the N_{bc,Al} might be attributed to an increase in positive effective-fixed-charges due to the defects induced by ion-implantation for buried channel layer.

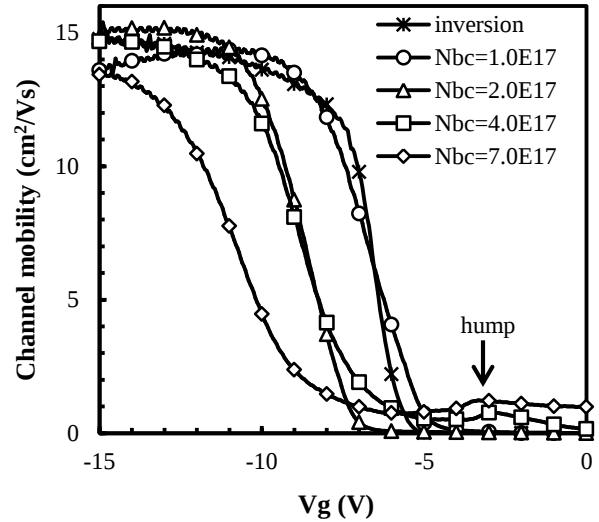


Fig. 3. Channel mobility of 4H-SiC p-channel MOSFETs with/without buried channel as a function of V_g.

4. Conclusions

We have investigated the effects of buried channel structure on channel properties of 4H-SiC(0001) n- and p-channel MOSFETs. For SiC n-channel MOSFETs, the channel mobility increased and threshold voltage decreased as the doping concentration of buried channel layer increased. These results suggest that we can control the channel properties of n-channel MOSFETs by buried channel structure. For SiC p-channel MOSFETs, however, the channel mobility was almost constant independently on the doping concentration of buried channel layer. The threshold voltage rather increased as the buried channel concentration. These results might be related to the low carrier density at the implanted buried channel layer due to the large ionization energy of acceptors and/or low mobility of the implanted buried channel layer. The difficulty to control the channel properties of SiC p-channel MOSFETs was revealed.

References

- [1] M. Okamoto, M. Tanaka, T. Yatsuo and K. Fukuda: Appl. Phys. Lett. Vol. 89 (2006), p. 023502-1
- [2] M. Okamoto, T. Yatsuo, K. Fukuda and H. Okumura: Jpn. J. Appl. Phys. Vol. 48 (2009), p. 04C087