Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp632-633

Step-stress Reliability Studies on AlGaN/GaN HEMTs on Silicon with Buffer Thickness Dependence

A. Frank Wilson*, Akio Wakejima, S. Lawrence Selvaraj and Takashi Egawa

Research center for Nano-Device and System, Nagoya Institute of Technology
Gokiso-cho, Showa-Ku, Nagoya 466-8555, Japan, *e-mail: wilson008@gmail.com

1. Introduction

Though many substrates are reported suitable for the growth of AlGaN/GaN heterostructure, undoubtedly silicon is the promising choice of substrate for its low cost and large size availability [1]. In-spite of extra ordinary performance, AlGaN/GaN HEMTs (GaN HEMTs) still needs investigation for reliability. Improvement in reliability requires a better understanding of failure mechanisms of GaN HEMTs which is essential [2]. GaN HEMTs with epi-layer total thickness (T_{tot}) of 3.5 µm and 5 µm. were step-stressed under increasing voltage.

2. Experiment

100 nm-thick SiO_2 passivated GaN HEMTs on silicon with T_{tot} of 3.5 µm and 5 µm (Fig. 1) were studied. The super lattice structured (SLS) buffer comprising multiple pairs of GaN/AlN (20/5 nm). The aluminum composition 26% and thickness 25nm are same for AlGaN barrier layer in both the HEMT structures with $L_g/L_{gd}/W_g$ of 1.5/4.0/200 µm.

Typical DC characteristics of both devices are listed in Table I. The fabricated devices showed good I_D-V_D characteristics with excellent pinch off.

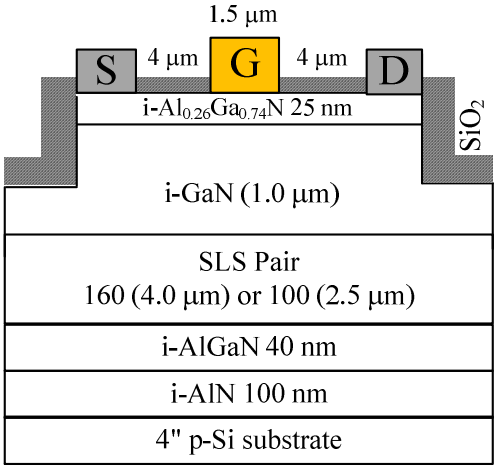

Fig.1. Device Structure of AlGaN/GaN HEMTs on silicon of buffer thickness 4.0 µm and 2.5µm with i-GaN of 1µm.

Table I. Device characteristics of AlGaN/GaN HEMTs on silicon.

SLS Pair	100	160
T_{tot} in [µm]	3.5	5.0
W_g [µm]	200	200
I_{Dmax} [mA/mm]	165	168
g_{mmax} [mS/mm]	58	70
V_{th} [V]	-1.66	-1.31

In step-stress measurement the gate bias was maintained at a V_g = -10V, a bias well below the threshold voltage. At this gate bias, V_D was varied from 20 V to higher bias until breakdown. Under these conditions, the device was stressed for 10 mins and I_D-V_D characteristics were measured every time before and after the step-stress.

3. Results and Discussion

For GaN HEMTs on T_{tot} = 3.5 µm, during 600 sec step-stress, no sudden increase in drain leakage was observed until 120V V_D stress. However, during V_D stress at 140 V, a sudden increase (≈2 orders) in the leakage current was observed as shown in Fig. 2.

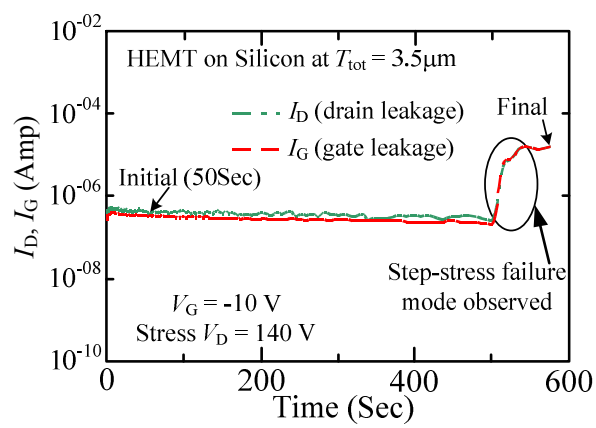

Fig. 2. Step-Stress measurement on T_{tot} = 3.5 µm at V_G = -10 V, V_D = 140 V stressed for 600 sec.

After 140 V_D stress, the I_D–V_D measurement showed a normal pinch off. This sudden increase in the leakage currents I_D, I_G, followed by good pinch-off I_D–V_D characteristics by the same device is what we mean as step-stress failure mode (*SSFM)*. For GaN HEMTs on T_{tot} = 5.0 µm no sudden increase in the I_D was observed. At a higher V_D stress total device breakdown was observed at 230 V without showing a *SSFM* as shown in Fig. 3.

At every increase in V_D stress the drain leak age is plotted as initial and final as shown in Fig. 4. The result shows and confirms the *SSFM* observed in Fig. 4(a) and the gradual increase in drain leak without *SSFM* is observed in Fig. 4(b).

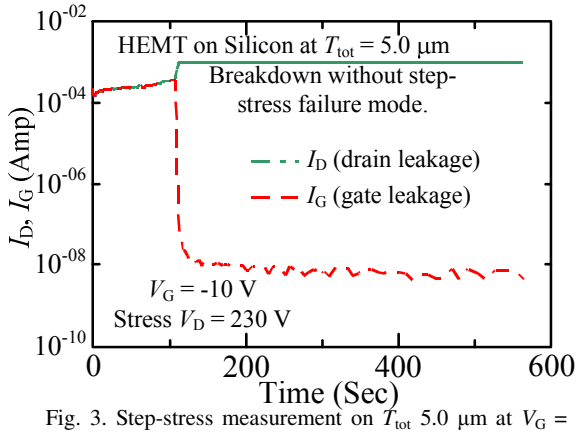

Fig. 3. Step-stress measurement on T_{tot} 5.0 µm at V_G = -10V, V_D = 230V stressed for 600 sec. Here the breakdown occurs without observing *SSFM*.

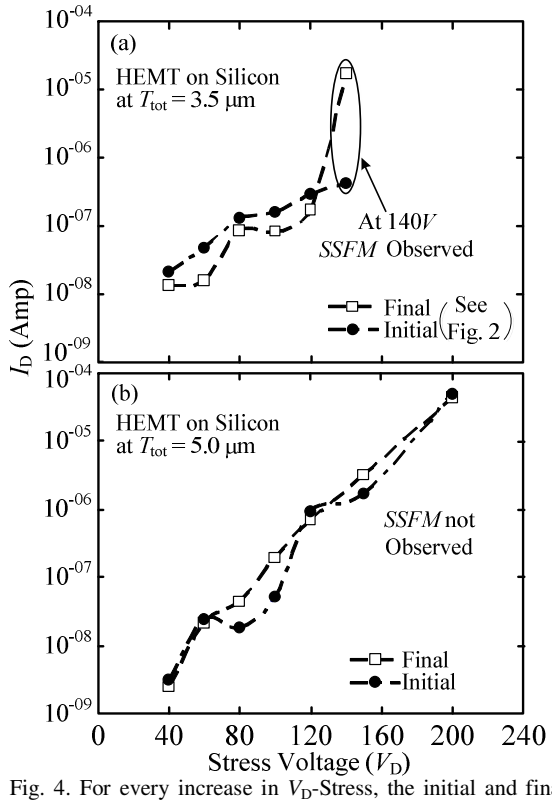

Fig. 4. For every increase in V_D-Stress, the initial and final point is plotted. SSFM observed for (a) T_{tot} 3.5 µm, however *SSFM* not observed for (b) 5.0 µm.

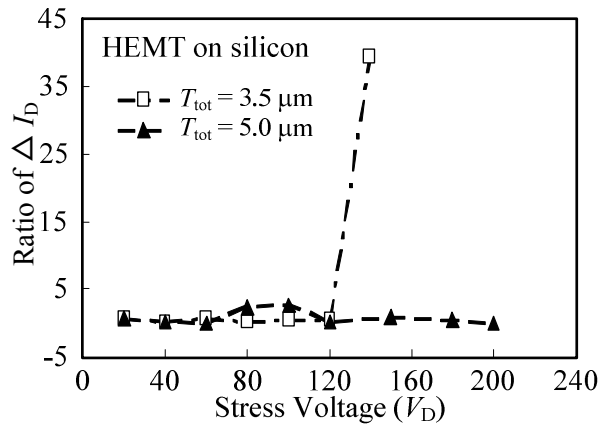

Fig. 5. The change in the drain leakage for$\Delta I_D = (I_{Final} - I_{Initial})/ I_{Initial}$. The T_{tot} = 5.0 µm shows a stable ID leak but in T_{tot} = 3.5 µm there is a sudden increase observed which is the *SSFM*.

Even though the drain leakage for T_{tot} = 5.0 µm increases (Fig. 4(b)), the ratio in drain leakage is calculated (i.e., $\Delta I_D = (I_{Final} - I_{Initial})/ I_{Initial}$) demonstrate a stable drain leakage, indicating no *SSFM*. On the contrary T_{tot} = 3.5 µm shows the sudden increase as shown in Fig. 5, which is *SSFM*.

4. Conclusion

We observed two types of failure mode under biasing stress conditions using GaN HEMTs grown on silicon of total thickness (T_{tot}) 3.5 µm and 5 µm. For GaN HEMTs on T_{tot} = 3.5µm, continuous biasing at 140 V caused a *SSFM*. On the contrary in the case of GaN HEMTs on T_{tot} = 5.0 µm no trace of *SSFM* identified even beyond 140V V_D stress but it ends in a permanent failure of device.

References

[1] S.Lawrence Selvaraj, Takaaki Suzue and Takashi Egawa, *IEEE Electron Device Letters*, 2009, pp.587.

[2] J. Joh and J. A. del Alamo, *IEDM Technical Digest*., 2006, pp.415.