Three Terminal Nano-Scale Electrode for Molecular Transistor Evaluation

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1. Introduction
With the advancement of computational technology, human beings have already reached 10P-FLOPS era, and E-FLOPS computers are expected within few decades, where extremely low power, high speed logic and high density memory devices are indispensable [1]. Single molecule devices, such as MOSES (Molecular Single Electron Transistor) [2-4] should be one of the most expected candidate devices which meet the above advanced requirements. However, nano-scale three terminal electrodes have not been accomplished yet, which are essential for evaluating the basic characteristics of the nano-scale transistors, although the concept of single molecule device was first demonstrated several decades ago [5], followed by the experimental demonstration of photoelectric conversion characteristics of molecular diode [6], and many evaluation results of two terminal single molecule devices have been reported [2-4], as well as two terminal nano-scale electrode technologies are reported [7,8]. This paper describes the fabrication technologies of three terminal nano-scale electrodes using electron beam lithography and lift-off technology. A 10 mm square chip was fabricated on which 288 three terminal nano-scale electrodes were fabricated, and the open resistance of which was in the order of 100 G ohms.

2. Fabrication Technologies
Fabrication technologies of three terminal nano-scale electrodes are schematically shown in Fig. 1. A 100 mm diameter silicon wafer was used as a substrate. A 200 nm thick silicon dioxide layer was thermally grown, and the surface was chemically cleaned. Electron beam sensitive resist (1) and (2) were applied onto the wafer to a thicknesses of 40 nm and 80 nm, respectively (a). Then, electron beam lithography by Elionix 7700 electron beam lithography machine defined the three terminal nano-gap structures. After development (b), a 30 nm thick gold layer was deposited onto the wafer by electron beam evaporation (c). Finally, the resist layers (1) and (2) were removed to lift-off the unnecessary part of the gold layer to fabricate the three terminal nano-scale electrodes.

3. Fabricated Chips
Optical and scanning electron microscope (SEM) image of the fabricated chip are depicted in Fig. 2. The chip size measures 10 mm square, and 6x6=36 sub-chips are placed in the central area of the chip, each of which contain 8 three terminal nano-scale electrodes, thus total of 36x8=288 three terminal nano-scale electrodes were fabricated on a chip.

As indicated in the figure, the gap lengths between electrodes are in the order of 15 nm, which would be small enough to evaluate molecular transistors, such as MOSES. In addition, it has to be noted that no sidewall were observed in the nano-scale electrode structures, due to the clever choice of resist (1) and (2), because the gap between electrodes measures less than 20 nm, while the thickness of...
the total resist exceed 100 nm, which indicates that the aspect ratio well exceed 5, which conventional technology cannot achieve. An atomic force microscope (AFM) image of the three terminal nano-scale structure is shown in Fig. 3. No sidewall is found around the electrodes, which indicate that the novel double layer resist system developed here offers quite reliable electrode structures. It also depicts that the thickness of the electrodes is about 29 nm, which coincide well with the designed value of 30 nm.

4. Electrical Evaluation of the Fabricated Chips

The electrical characteristics of the fabricated three terminal nano-scale electrodes were evaluated, and the results indicate that the resistance between two of the three electrodes well exceed 100 G ohms. The maximum breakdown voltage between the electrodes is around 10 V, or more than 0.5 V/mm, which would be high enough for planar electrode structure on silicon dioxide surface, considering that the highest bulk insulator breakdown field is in the order of 1 V/mm. In addition, since the thickness of the nano-scale electrode is around 30 nm, the resistance is almost negligible in evaluating single molecule devices. Thus, this three terminal nano-scale electrodes should be the platform for evaluating single molecule three terminal devices, such as MOSES. Since the electrode material can be arbitrarily chosen among those evaporable metals and conductors, even magnetic or strongly correlated nano-scale three terminal devices can be evaluated using this chip. Therefore, this nano-scale electrode chip would be the platform for evaluating three terminal nano-scale devices, and should pave the way towards the single molecule/nano-scale device era.

5. Conclusion

Novel fabrication technologies of three terminal nano-scale electrode, with less than a 20 nm gap were demonstrated, which would enable to quantitatively evaluate three terminal single molecule devices, such as MOSES, and to pave the way to an P-FLOPS one chip super processor and E-FLOPS supercomputer in the near future.

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References