Room temperature fabrication of HfON gate insulator for low-voltage operating pentacene-based organic field-effect transistors

Min Liao 1, Hiroshi Ishiwara 1,2, and Shun-ichiro Ohmi 1

1 Department of Electronics and Applied Physics, Tokyo Institute of Technology, J2-72, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
Phone: +81-45-924-5473, E-mail: liao.m.aa@m.titech.ac.jp, ohmi@ep.titech.ac.jp

2 Department of Physics, Division of Quantum Phases and Devices, Konkuk University, Seoul 143-701, Korea

1. Introduction

In addition to carrier mobility, subthreshold swing (SS), threshold voltage ($V_{th}$) and off/on current ratio ($I_{on}/I_{off}$) must also be optimized to ensure proper operation of the organic field-effect transistors (OFETs). Although annealing of high-k gate insulators in an inert atmosphere can enhance the carrier mobility and improve the SS of OFETs, the high annealing temperature restricts their application in flexible organic devices [1, 2]. Interestingly, the employment of HfON gate insulator can realize superior interface properties in oxide thin film transistors and OFETs, thereby considerably improving their electrical properties [3, 4].

In this paper, we report on the fabrication and characterization of pentacene-based OFET with room-temperature-processed HfON gate insulator.

2. Experimental Procedure

Pentacene-based OFETs were fabricated on n$^+$-Si(100) substrates with a top-contact bottom-gate device geometry, as shown in Fig. 3 (a). HfON gate insulators were deposited by electron cyclotron resonance (ECR) plasma sputtering at room temperature [5]. Then, pentacene films (20 nm) were deposited on HfON gate insulators by thermal evaporation method at 70°C (2.0x10$^{-6}$ Torr, 0.01 nm/s). Au electrodes were evaporated through a shadow mask to form source and drain electrodes for OFETs. The channel widths (W) and lengths (L) of the fabricated OFETs were 500/50, 500/100, 500/200 and 500/300 μm, respectively. Meanwhile, Au/HfON/n$^+$-Si(100) capacitor was fabricated to evaluate the capacitance and leakage current density of the gate insulator. All measurements were carried out in air.

3. Results and Discussion

The C-V and J-V characteristics of the Au/HfON/n$^+$-Si(100) capacitor are shown in Fig. 1. The Au/HfON/n$^+$-Si(100) capacitor shows a low leakage current density of 7x10$^{-7}$ A/cm$^2$ at a gate voltage of -2 V. The capacitance (C) at a gate voltage of -2 V is 1.05 μF/cm$^2$, which yields a capacitance equivalent thickness (CET) of 3.4 nm. Figure 2 shows the AFM image of the room-temperature-processed HfON gate insulator. The root-mean-square (RMS) roughness value of the fabricated HfON gate insulator is 0.54 nm. It is lower than that of other high-k gate insulator [6, 7] or even comparable to that of the polymer/high-k hybrid gate insulator [7].

Figure 3 shows the schematic of OFET and the $I_D$-$V_G$ characteristics of the fabricated OFETs with room-temperature-processed HfON gate insulators at different channel sizes. One can see that the maximum drain current increases with increasing W/L ratio. The OFET with channel W/L=500/50 μm shows the highest maximum drain current, leading to a large $I_{on}/I_{off}$ ratio of 1x10$^5$. $V_{th}$ and SS of the OFET with channel W/L=500/50 μm are -0.4 V and 0.13 V/decade, respectively.

It is known that the electrical properties of OFETs do not only depend on active layer morphology but also depend on the contact resistance ($R_{C}$) of the electrodes to the semiconductor layers. The $R_{C}$ can be extracted by the transfer line method (TLM) [8]. Figure 4(a) shows the width-normalized total resistance ($R_{total}$) as a function of the channel length for the OFETs with a channel width of 500 μm. Based on the slope of the lines in Figure 4(a), the intrinsic hole mobility for the pentacene channel layer is estimated to be 0.6 cm$^2$/Vs, about 2.3 times higher than the hole mobility (0.26 cm$^2$/Vs) of the OFET with the channel W/L=500/50 μm. Figure 4(b) shows the width-normalized contact resistance and the width-normalized channel resistance ($R_{C}$) as a function of gate voltage for the OFET at the channel W/L=500/50 μm. It is found that the $R_{C}$ of the OFET with channel W/L=500/50 μm is higher than the $R_{C}$. However, the effect of contact resistance on the electrical properties becomes weaker when the channel length becomes longer, because the channel resistance is becoming the dominant contributor to total resistance of OFET (see Fig. 4(a)). Therefore, the mobility of pentacene based OFETs with room-temperature-processed HfON gate insulator increases with channel length, leading to a mobility of 0.38 cm$^2$/Vs for the OFET with channel W/L=500/300 μm, as shown in Fig. 4 (c).

4. Conclusion

Pentacene-based OFETs with room-temperature-processed HfON gate insulator have been fabricated and characterized. Due to the excellent interface properties and good electrical properties of HfON, the OFET with the room-temperature-processed HfON gate insulator shows good electrical properties.

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References

Fig. 1  (a) Schematic of Au/HfON/n^+-Si(100) capacitor, (b) C-V (10 kHz), and (c) J-V characteristics of the capacitor.

Fig. 2  AFM image of the room-temperature-processed HfON gate insulator (1 μm x 1 μm, z: 5 nm/div.).

Fig. 3  (a) Schematic of the pentacene-based OFET, and (b) I_D-V_G characteristics of pentacene-based OFETs with room temperature processed HfON gate insulator at different channel sizes.

Fig. 4  (a) Width-normalized total resistance as a function of the channel length for the OFETs with a channel width of 500 μm, (b) width-normalized contact resistance and width-normalized channel resistance as a function of gate voltage for the OFET at the channel W/L=500/50 μm, and (c) hole mobility of OFETs as a function of channel length.