

# Organic Thin-Film Transistor-Based Non-Volatile Memory Devices

Jang-Sik Lee

Kookmin Univ.  
School of Advanced Materials Engineering  
Seoul 136-702, Korea  
Phone: +82-2-910-4288 E-mail: jangsik@kookmin.ac.kr

## 1. Introduction

Much progress has been done on semiconductor devices that are based on organic materials for flexible/printed electronic device applications [1]. These organic devices can be processed at low temperatures and low costs, and, therefore, are regarded as one of the most important types of semiconductor devices for future flexible/stretchable electronic device applications. Most of these studies have focused on the transistors and the logic circuits based on organic material components, and currently, transistor devices and logic circuits with excellent electrical performance can be fabricated. Memory devices, however, must be integrated with the transistors and logic circuits in future flexible electronic devices, and organic transistor-based nonvolatile memory devices are viable candidates for these electronic devices because it is feasible to adopt the advanced organic transistor device technology for fabrication of high-performance organic memory devices. Thus, the existing organic electronic components (transistors, logic circuits, etc.) can easily be integrated with organic transistor-based memory devices for embedded device applications. Especially, organic transistor-based nano-floating gate memory device is one of the best candidates for future system-on-chip flexible/printable electronic devices [2-4]. The device structure and operation scheme are similar to those of conventional flash memory devices, so the existing advanced flash memory technology can be used and the scaling to high-density memory devices will be feasible.

In this presentation recent progress in organic transistor-based nano-floating gate memory devices will be discussed as future memory devices for organic electronic devices.

## 2. Device Structures

The schematic device structures and basic operation scheme of non-volatile flash memory devices are shown in Fig. 1. In case of conventional flash memory devices the charge storage layer is a floating gate. Floating gate is highly-conductive polycrystalline silicon and thus the charge storage layer is continuous. Recently, active research has been done on the fabrication of flash memory devices by using discrete charge trapping layers, for example, silicon nitride and metallic/semiconducting nanocrystals. This memory structure has an advantage over conventional flash memory devices in terms of robust data retention, immunity to capacitive coupling, etc.

In case of nanocrystal-based flash memory devices (called nano-floating gate memory) conventionally the nanocrystals are formed at high temperatures, so it is very difficult for those nanocrystals to be used in organic memory devices. However, it has been reported on the synthesis of low-temperature processed nanocrystals and their applications to organic memory devices. The basic operation scheme for flash-type memory devices is simple. In the case of MOS transistor devices, the threshold voltage ( $V_{th}$ ) is fixed at a constant drain voltage ( $V_d$ ). On the other hand, non-volatile memory devices have charge storage (or trapping) layers, so the charge carriers can be stored (or trapped) in the charge storage layer. A conventional flash memory cell has a floating gate, so the electrons can be stored in the floating gate by the programming operations and moved back to the substrate by the erasing operations. According to the programming/erasing operations,  $V_{th}$  can be changed since channel conductance is influenced by whether the charge carriers are stored in the floating gate or not. Thus, one can verify the programmed and erased states of the flash memory devices by measuring the drain current ( $I_d$ ). The erased and programmed states are "1" and "0" states, respectively. Therefore, each flash memory cell can store information as either "0" or "1". Advanced flash memory technology can store more than 1 bit in each flash memory cell, making it possible to increase the memory density further without reducing the cell size. The stored charges are located in the potential well of blocking (also known as the control oxide) and tunneling oxide layers, so the information can be maintained even after the power outage, resulting in non-volatility. This is the major technical advancement that has been made since the invention of flash memory devices using the floating gate [2,4].

## 3. Organic Thin-Film Transistor-Based Non-Volatile Memory Devices

Recently, many studies have been conducted regarding the use of organic semiconductors as the active layer in transistor-based nano-floating gate memory devices. In this type of memory devices several key device components exist. First is the semiconductor layer. Normally, pentacene is used as the active layer. Otherwise, many organic semiconductor materials, for example, poly(3-hexylthiophene) (P3HT), copper phthalate

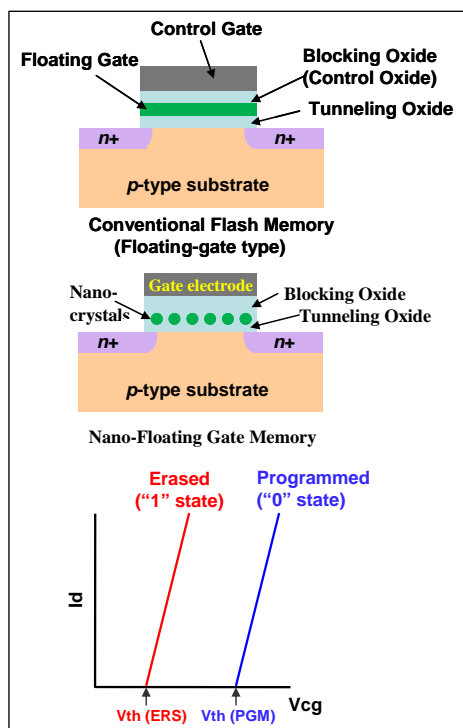


Fig. 1 Schematic device structures for non-volatile memory devices based on floating gate and nanocrystals. Typical programmed/erased states were illustrated.

cyanine (CuPc), etc. can be used. Since the performance of organic thin-film transistor (OTFT)-based nano-floating gate memory devices is directly related to the performance of OTFTs, it is crucial to obtain high-performance OTFT performance for better memory operations. Second, the dielectric layer is very important. In contrast to the OTFTs OTFT-based nano-floating gate memory devices should use two dielectric layers, one for blocking and the other for tunneling dielectric layer. Good insulating properties ensure the good data retention, so it is very important to choose proper dielectric materials. Actually, electrical/dielectric properties, for example, the bandgap, dielectric constant, leakage current, etc. are directly related to the memory operations, so many efforts have been done on the development of good dielectric materials for OTFT-based nano-floating gate memory devices. Many studies have used the inorganic materials, for example,  $\text{SiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , etc. Inorganic dielectric materials can give us better electrical properties than organic dielectric materials, so good memory performance has been reported by using those materials. For future flexible device applications it is highly required to use organic dielectric materials. Thus, recently, many studies are reported on the fabrication of OTFT-based nano-floating gate memory device by utilizing organic dielectric layers. Poly(methylmethacrylate) (PMMA), polyimide (PI), poly 4-vinylphenol (PVP) are typically used organic dielectric layers. Third is the charge trapping layer. Actually, this is one of the most

important device elements in OTFT-based nano-floating gate memory devices. There are various ways to synthesize these metallic nanoparticle-charge trapping elements. Similarly, many kinds of metallic nanoparticles have been applied to nanoparticle-based memory devices. The synthesized metallic nanoparticles should be attached to the desired surface on the substrates. The charge trapping layer is formed in most cases by the self-assembly process. One can synthesize a metallic nanoparticle layer by depositing very thin metallic layers. After depositing the thin metallic layer, a post-annealing process is performed in order to synthesize agglomerated metallic nanoparticles. On the other hand, active research has been undertaken in the field of nanoparticle-based memory devices using colloidal metallic nanoparticles. In this field, the synthesis of metallic nanoparticles can be done in solution, and there is no need for post-deposition annealing to form metallic nanoparticles. In addition, one can control the size of the metallic nanoparticles very easily. Another important advantage of using solution-processed metallic nanoparticles as the charge trapping layers lies in the fact that this process can be done at very low temperatures. The solution-processed metallic nanoparticles should be attached to or adsorbed on the desired surface of the substrates. Typically, their adsorption can be achieved by the electrostatic interaction between the metallic nanoparticles and the adhesion layers. The immobilization of the metallic nanoparticle layer is said to be achieved via the surface modification of the substrates [2,4,5].

#### 4. Conclusions

Much progress has been done on OTFT-based nano-floating gate memory devices through the active researches for fabrication of high-performance memory devices. The fabrication processes have been optimized to get the best device performance. In this presentation the recent research activities related to fabrication of high-performance OTFT-based non-volatile memory devices will be reviewed in detail.

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