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Variation of Active Layer Thickness of Polymer Thin Film Transistors and its Effect on Digital Circuits Performance

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1. Introduction

For the last years organic materials have received increased attention for their application in electronic devices and circuits. Organic thin films transistors (OTFTs) are gaining attention as a technology that enables electronic circuits to be fabricated using low-cost processing. Polymeric TFTs (PTFTs) are been intensively studied, with poly(3-hexyl-thiophene) providing high mobility values as well as other advantages with respect to other polymers. Simulation of devices and circuits requires an accurate model to represent the behavior of the device. Some authors have used simulation in SPICE using the MOSFET model, to which some features as series and nonlinear resistance at drain and sources are sometimes added.

However, less attention has been dedicated to the optimization of device geometry for a more efficient device operation, where the thickness of the active layer (tS) has been reported to affect in different ways device characteristics.

In this work we report and analyze the link between transistor behavior when active layer thickness is varied and the digital circuit performance.

2. Experimental

Using our unified model and parameter extraction method (UMEM), the values of model parameters were extracted from transfer and output characteristics of PTFTs with different active layer thicknesses, TableI.

Table I. Model parameters extracted of PTFTs with different active layer thickness.

tS [nm]	λ [1/V]	α	R [Ω]	m	VT [V]
20	-1.617x10-3	0.484	5.863x105	1.571	3.517
30	-1.096x10-3	0.456	8.373x105	1.619	5.031
40	-4.136x10-4	0.429	9.157x105	1.693	6.353
80	-5.024x10-4	0.431	9.496x105	1.675	6.815
120	-5.646x10-4	0.433	9.454x105	1.665	6.932

After that, the PTFT expressions model eq. (1) [2], were introduced in SMASH AMS simulator [1], using Verilog-A language in order to obtain the electrical characteristics of PTFTs.

$$I_{DS} = \frac{W}{L}\cdot Ci\cdot \mu_{FET}\cdot \frac{(V_{GS}-V_T)\cdot(1+\lambda\cdot V_{DS})}{\left(1+R\cdot\frac{W}{L}\cdot Ci\cdot\mu_{FET}\cdot(V_{GS}-V_T)\right)\cdot\left(1+\left(\frac{V_{DS}}{\alpha\cdot(V_{GS}-V_T)}\right)^m\right)^{\frac{1}{m}}} \quad (1)$$

To verify the relevance of our model, it has been tested with experimental PTFTs, Fig. 1.

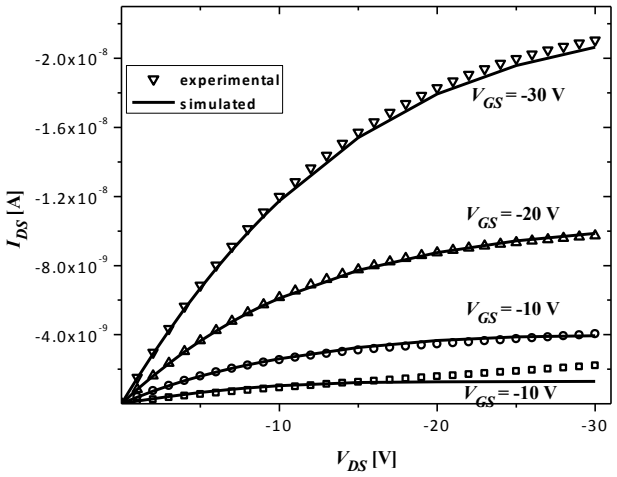

Fig. 1. Experimental and simulated characteristics of transistors with 80 nm of P3HT active layer thickness.

The output characteristics of PTFTs with a P3HT active layer of 20, 30, 40, 80 and 120 nm, simulated in SMASH with the extracted parameters indicated above are shown in Fig. 2, for V_{GS} = 0 V. It can be observed that the drain current increases with the P3HT thickness.

It is worth to remark, that for this device, the $I_{DS} - V_{DS}$ curve for V_{GS} = 0 a drain current is present due to the conductivity of the P3HT layer between drain and source, which depends on the non-intentional doping of the active layer and this effect is much more pronounced for devices with P3HT thickness above 80 nm.

A single inverter circuit using two p type PTFTs was simulated. A conventional p-type "diode-load" inverter is constituted of one driving transistor and a load transistor, Fig. 3.

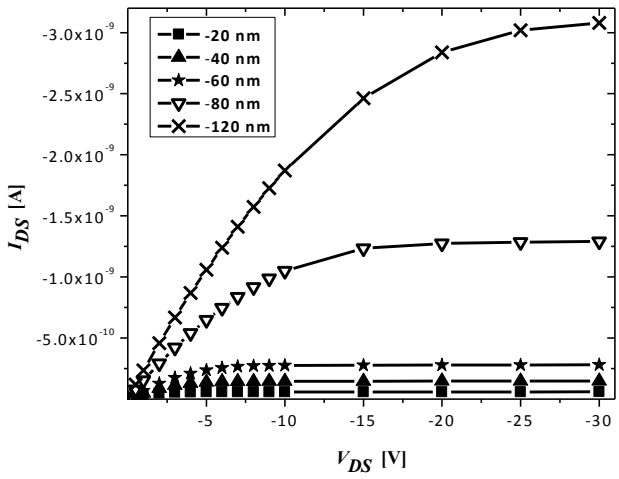

Fig. 2. Simulated PTFT output characteristics for VGS = 0 V with different active layer thickness.

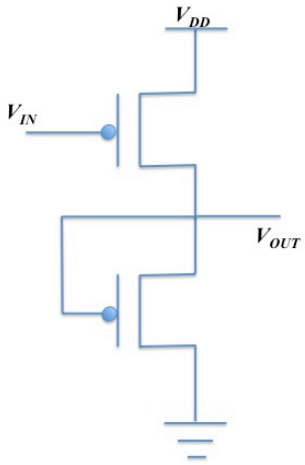

Fig. 3. Polymer diode-load inverter.

Simulated transfer characteristics of inverter circuit using load and driver PTFTs with the same active layer thickness and $r_W = 10$ are shown Fig. 4.

To ensure the correct operation of the digital circuit, one has to take into account some stability considerations. The noise margin (NM) of an inverter is an important figure of the stability of the digital circuits. We will analyze the influence of the active layer thickness on the noise margin and gain (dV_{OUT}/dV_{IN}).

We can compare how the noise margin depends on P3HT thickness. This evaluation give up that decreasing the thickness of P3HT layer can increase the noise margin, the high noise margin was found by 20 nm, Table II. The maximum gain also has been obtained by the same thickness, but these results are low and are related with drain-source current when V_{GS} = 0 V and the low on/off ratio show for these transistors [3].

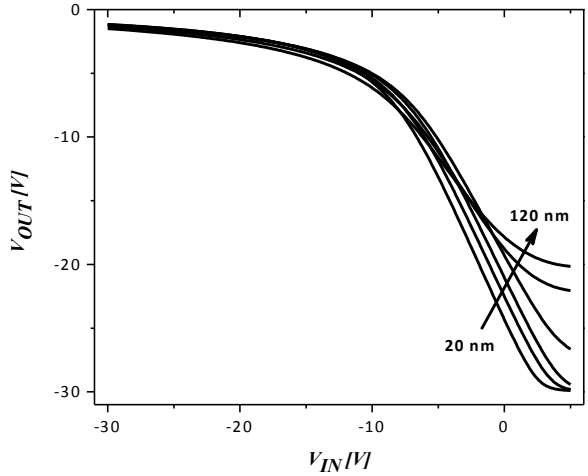

Fig. 4. Transfer characteristics of "diode-load" inverter with different active layer thickness.

Table II. Noise margin and maximum gain calculated for "diode load" inverter with different active layer thickness

t_S [nm]	NM	A
20	0.81	2.28
30	0.49	2.20
40	0.26	2.13
80	0.10	1.62
120	0.03	1.40

3. Conclusions

A compact model of PTFTs using Verilog-A language was implemented in SMASH simulator. Transfer characteristics of an inverter circuit were obtained, which was used to analyze the effect on them of the variation of PTFT active layer thickness. Results were validated using measured characteristics of PTFTs fabricated with PMMA on P3HT. Results show that decreasing the thickness of P3HT layer can increase the noise margin, the higher noise margin was found by thick of layer lower than 40 nm, these data are related with drain-source current when V_{GS} = 0 V and the low on/off ratio show by these transistors.

Acknowledgements

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