

Control of switching voltage of low voltage organic complementary inverter using floating gate structure

Tomoyuki Yokota¹, Tsuyoshi Sekitani², Takashi Nakagawa¹, Yoshiaki Noguchi¹, Ken Takeuchi², Ute Zschieschang³, Hagen Klauk³, and Takao Someya^{1,2,4}

¹Applied Physics, University of Tokyo,
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan

Phone: +81-3-5841-6756 E-mail: yokota@ntech.t.u-tokyo.ac.jp

²Electrical and Electronic Engineering and Information Systems, University of Tokyo,
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan

³Max Planck Institute for Solid State Research,
Heisenbergstrasse 1, 70569 Stuttgart, Germany

⁴Institute for Nano Quantum Information Electronics (INQIE), University of Tokyo,
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan

1. Introduction

Organic thin-film transistors (TFTs) have recently attracted much attention since their inherent mechanical flexibility and durability are suitable for realizing large-area flexible electronics such as robotic sensory arrays [1], e-paper [2] and RFID tags [3]. In these applications, it is important to reduce power consumptions of organic TFTs. One of the straightforward approaches to achieve it is to exploit complementary circuit layouts consisting of TFTs with the low operation voltages. Although many organic complementary inverter circuits have been reported [4], the reducing of the operation voltage degrades the yield and/or performance dispersion of the inverter.

One of the approaches to solve this problem is the threshold voltage control of the organic transistor. Recently, several approaches to control threshold voltage such as surface modification of the gate dielectric with a self-assembled monolayer (SAM) [4,5]. This approach, the threshold voltage of the transistors can be set to a specific value during manufacturing. On the other hand, it is very important to control the threshold voltage after manufacturing, since the threshold voltage of organic transistors is changed inadvertently during operation due the DC bias-stress effect and air exposure. Previously, the double-gate structure [6] has been used to control the threshold voltage of organic TFTs after manufacturing. However, this structure was impossible in low operational TFTs because the operational voltage was very large.

In this study, we demonstrate the threshold-voltage control of low-voltage organic TFTs with a floating-gate structure after manufacturing, which allows us to control the behavior of low-voltage organic complementary inverters during operation.

2. Fabrication process

The cross-sectional illustration and optical microscope image of the organic complementary inverter circuits are shown in Figure 1. These transistors are fabricated by vacuum evaporation and solution processes. First, 25-nm-thick Al layer is thermally evaporated through a

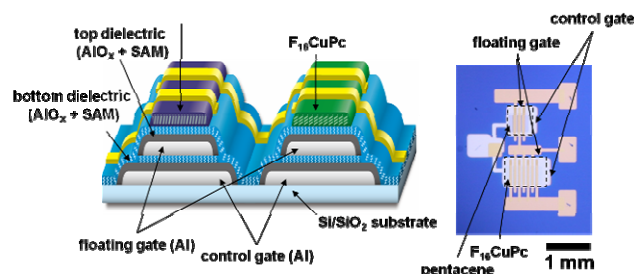


Fig. 1 (a)The cross-sectional illustration of the organic CMOS inverter circuits. (b)The optical microscope image of organic CMOS inverter circuits.

shadow mask as control gate. Second, we form control gate dielectric layers. Then 25-nm-thick Al layer is evaporated on the control gate dielectric layers and formed floating gate dielectric layers. The control and floating gate dielectric layers consist of thin layers of aluminum oxide and molecular SAMs. A thin aluminum oxide layer is formed by oxygen-plasma treatment and a SAM layers are prepared from a 2-propanol solution containing 5 mM of n-octadecylphosphonic acid for 16 hours at room temperature. Purified pentacene and F₁₆CuPc are deposited in vacuum through a shadow mask to form a 50-nm-thick as p- and n- type organic semiconductors on the floating gate dielectric layer. Finally, a 50-nm-thick Au layer is evaporated through a shadow mask to form the source and drain electrodes.

3. Results

Fig. 2 shows transfer characteristics of fabricated organic transistor with channel length and width of 50 μm , 3500 μm respectively. Each transfer characteristics were measured after programming. The programming voltage bias of the control gate electrode of the p-type transistors is applied from 0 to -6 V and that of n-type transistors is applied from 0 to +6 V for 1 second respectively. In fig 3, the threshold voltage of p- and n-type transistors plotted as a function of programming voltage. The threshold voltages of the p- and n-type transistors are changed

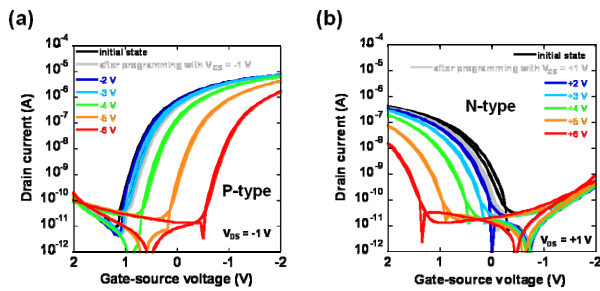


Fig. 2 Transfer characteristics of the pentacene and F₁₆CuPc TFTs with channel length of 50 μm and channel width of 3500 μm . (a) Transfer characteristics of pentacene TFTs recorded after program operations performed with program voltages ranging from -1 V to -6 V. (b) Transfer characteristics of F₁₆CuPc TFTs recorded after program operations performed with program voltages ranging from 1 V to 6 V.

systematically within wide ranges from $+2.4$ to -1 V and from -0.3 to $+1.5$ V, respectively, when the programming voltage of the control gate electrode of the p-type transistors is applied from 0 to -6 V and that of n-type transistors is applied from 0 to $+6$ V. These threshold voltage windows are very large by comparison with the operation voltage of these transistors.

Then, figure 3 shows the electric characteristic of the fabricated CMOS inverter circuits. The pentacene transistor has a channel width of $1000 \mu\text{m}$, the F₁₆CuPc transistor has a channel width of $3000 \mu\text{m}$, and both transistors have a channel length of $50 \mu\text{m}$ in the inverter circuits. The inverter circuits operated with good characteristics at driving voltage of 1.5 V and with a signal gain larger than 10. Figure 4 shows the input-output characteristic of inverter circuits when the driving voltage is 1.5 V after applying to the control gate electrodes from -6 V to 6 V for 1 second. As the programming voltage goes to $\pm$ side, input-output characteristic is being shifted to more $\pm$ side of input voltage. This is because the threshold voltages of p- and n-type transistors have been changed by applying programming voltage to the control gate electrode. When the programming voltage is -6 V, the output voltage is almost 0 V against the input voltage between 0 V and 1.5 V. On the other hand, when the programming voltage is $+6$ V, the output voltage is almost 1.5 V against the input voltage between 0 V and 1.5 V. In this way, the input-output characteristic of inverter circuits was able to be controlled by changing programming voltage. Then, the gain is almost same for 10 after applying programming voltage.

4. Conclusions

In this work, we have fabricated floating gate organic transistors that operate with below 3 V by using SAM gate dielectrics. The threshold voltage of fabricated p-type and n-type organic transistors are controlled very wide range by applying programming voltages. Then, we have fabricated organic CMOS inverter circuits using these transistors. This

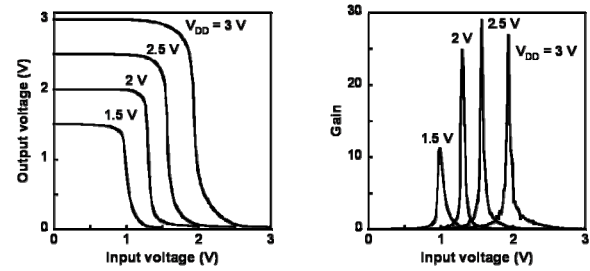


Fig. 3 Output voltage and small-signal gain as a function of input voltage for driving voltages between 1.5 and 3 V.

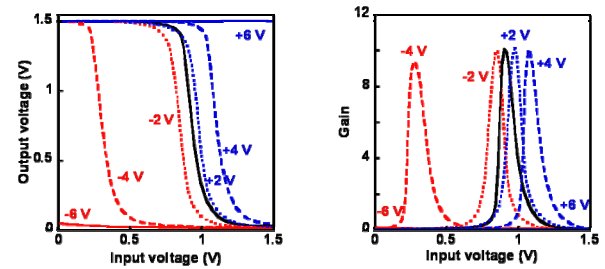


Fig. 4 Output characteristics of the inverter at a supply voltage of 1.5 V measured after program voltages between -6 V and $+6$ V had been applied to the input node for a duration of 1 s. The switching voltage is systematically controlled by the program pulses.

inverters were operated between 1.5 V and 3 V with a signal gain larger than 10 . We have been also able to control the threshold voltage of the inverter circuits by applying programming voltage to the control gate electrode.

In the future, this technology will be expected to apply the various new electronics by integrating this CMOS inverter in the logic circuits.

5. Acknowledgements

This work is partially supported by Special Coordination Funds for Promoting, JST/CREST and KAKENHI (Wakate S). One of the authors (T.Y.) is grateful to the research fellowships for young scientists of JSPS.

6. References

- [1] Y. Kato, T. Sekitani, Y. Noguchi, T. Yokota, M. Takamiya, T. Sakurai, and T. Someya, IEEE Trans. Electron Devices **57**, 995 (2010).
- [2] J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, and P. Drzaic, Proc. Natl. Acad. U.S.A. **98**, 4835 (2001).
- [3] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, App. Phys. Lett. **82**, 3964 (2003).
- [4] Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa and Y. Iwasa, Nat. Mater. **3**, 317 (2004).
- [5] K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid and G. Schitter, J. Appl. Phys. **96**, 6431 (2004).
- [6] K. Hizu, T. Sekitani, T. Someya, and J. Otsuki, Appl. Phys. Lett. **90**, 093504 (2007).