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3V-Operation Organic Transistors on Shape-Memory Film with Polyimide Planarization Layer

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1. Introduction

Organic thin-film transistors (OTFTs) have attracted much attention for an inherent characteristic of flexibility, which is exploited in applications such as sensor arrays attached to a curve surfaces[1], flexible displays[2,3] and RFID tags[4]. Because organic transistors are fabricated with low temperature process, various non-heat-resisting substrates such as plastic films are applicable.

However, it is difficult to fabricate high performance transistors on thin film substrates because the rough surface of the film inhibits the growth of semiconductor grains and reduces the mobility[5]. One solution is to form a planarization layer of polymer on the gate electrodes. The polymer layer also serves as gate dielectrics although the high operation voltage of 40 V is required due to the large thickness of the gate dielectrics as large as 500 nm[6].

In this study, we formed a planarization layer and gate dielectric separately. By using hybrid gate dielectrics of aluminum oxide and self-assembled monolayers (SAMs)[7], the operation voltage was decreased to as small as 3 V. As for the substrate, a shape-memory film was used. By forming a planarization layer in optimized condition, which reduces the surface roughness (root mean square (RMS) of atomic force microscopy) of 244 nm to 44 nm, the mobility of 0.51 cm^2/Vs was obtained. This film is applied to elastic circuit by forming into a helix after fabrication and heated to memorize its form at more than 150ºC and then cooled, which causes the substrate to permanently adapt the helical structure[8].

2. Fabrication process

The cross-sectional illustration of the organic transistor is shown in Fig. 1. Firstly, Polyimide was spin-coated at 2000 rpm for 2 minutes on the surface of the shape-memory film to form a planarization layer. Then the film was annealed in nitrogen flow as the temperature was increased; at 120°C, 150°C, 180°C in 1 hour sequence for each. Aluminum gate electrode with thickness of 350 nm was deposited by thermal evaporation onto the surface of

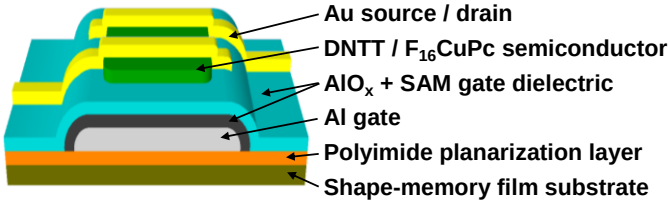

Fig. 1 Cross-sectional illustration of the device. Polyimide planarization layer was spin-coated. gate dielectric layers were fabricated with ashing process and dipping process. The others were evaporated.

planarization layer. As gate dielectristics, aluminum oxide film was formed by oxygen plasma ashing treatment (50W, 15 min) and SAM layer was formed by dipping the device into 2-propanol solution of 5 mmol/L n-octadecylphosphonic acid for 16 hours. Surface of the device was rinsed with pure 2-propanol and annealed in an oven at 100ºC for 10 minutes. Then organic semiconductor with thickness of 30-60 nm was deposited by thermal evaporation onto the gate dielectrics. Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene(DNTT)[9] was used as p-type semiconductor and hexadecafluorophthalocyanine(F_{16}CuPc) was used as n-type semiconductor. Finally gold source and drain electrodes with thickness of 200 nm were deposited by thermal evaporation onto the organic semiconductor.

3. Results

Figure 2 shows the AFM images of the surfaces of the substrates. RMS roughness was 244 nm for the substrate without a planarization layer while by spin-coating polyimide, the surface of the substrate was planarized; RMS roughness were 105 nm, 44 nm and 35 nm for spin-coating at 4000 rpm, 2000 rpm and 1000 rpm respectively. Because RMS roughness of 2000 rpm was almost equivalent to that of 1000 rpm, TFT performances of the two devices were almost equivalent.

Fig. 3 shows transfer characteristics and output characteristics of the fabricated organic transistors with channel

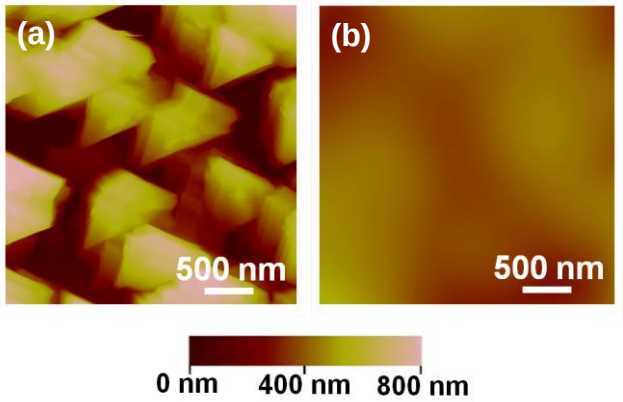

Fig. 2 AFM images of the surfaces of substrates. (a) Without planarization layer. RMS roughness is 244 nm. (b) With planarization layer spin-coated at 2000 rpm for 2 minutes. RMS roughness is 44 nm.

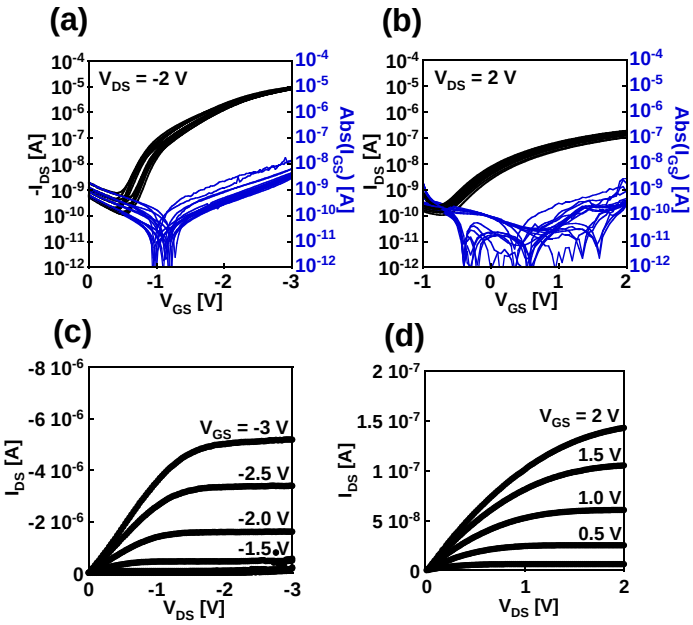

Fig. 3 Transfer characteristics and output characteristics of fabricated organic transistors with channel length of 40 µm and width of 500 µm. (a) Transfer characteristics of p-type transistors. The mobility is 0.51 cm^2/Vs and the on/off ratio is 4.6×10^4. (b) Transfer characteristics of n-type transistors. The mobility is 0.0073 cm^2/Vs and the on/off ratio is 9.7×10^2. (c) Output characteristics of a p-type transistor. (d) Output characteristics of an n-type transistor.

length of 40 µm and width of 500 µm. The mobility of p-type transistors was 0.51 cm^2/Vs while the mobility of the transistors on bare shape-memory film was 0.0045 cm^2/Vs.

Furthermore, we fabricated CMOS inverter circuits. Figure 4 shows the optical microscopic image of a CMOS inverter circuit and input output characteristics and signal gain of the inverter consisting of the p-type transistor with 30 µm channel length and 800 µm width and the n-type transistor with 30 µm channel length and 3200 µm width. The inverter circuits were operated at driving voltage between 1.0 V and 3.0 V. Signal gain was 92 at 3 V.

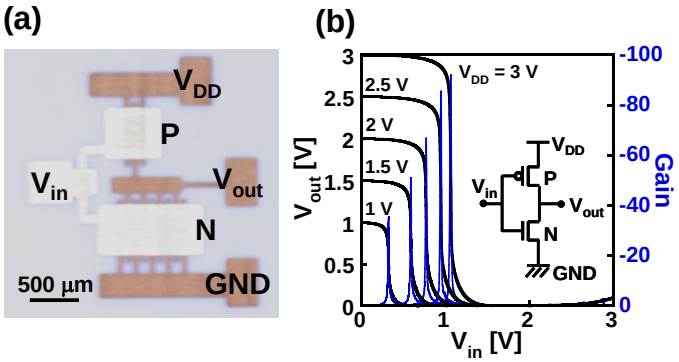

Fig. 4 (a) Optical microscopic image of organic CMOS inverter circuit. (b) Output voltage and signal gain of CMOS inverter circuit as a function of input voltage for driving voltages between 1.0 V and 3.0 V.

4. Conclusions

In this study, we have fabricated 3V-operation organic transistors and CMOS inverter circuits on a shape-memory film with rough surface by forming a polyimide planarization layer and hybrid gate dielectrics of aluminum oxide and SAM. By spin-coating polyimide, we have obtained plane surface with RMS roughness of as small as 44 nm in comparison with bare film of RMS roughness as large as 244 nm, and p-type transistors with the high mobility of 0.51 cm^2/Vs. Also CMOS inverter circuits were fabricated and operated with applied voltage between 1.0 V and 3.0 V, with the largest signal gain of 92 at 3 V.

Acknowledgements

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