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Solution-processed C_{60} field-effect transistors with high mobility

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1. Introduction

Carbon 60 fullerene, C_{60}, is a promising material that provides high filed-effect mobilities of more than 1 $cm^2 V^{-1} s^{-1}$ in the organic thin-film transistors (TFTs) [1,2]. C_{60} TFTs, which generally operate as an *n*-channel transistor, are useful to construct complementary circuits by use of them with *p*-channel organic TFTs such as a pentacene TFT [3,4].

Solution process for deposition of organic semiconductor in the TFT is desirable for low-coat process that is an advantage in organic TFT. Solution-processed *n*-channel organic TFTs with various C_{60} derivatives have been demonstrated [5-8]. The reported field-effect mobility ranges from 1.9×10^{-8} to 0.5 $cm^2 V^{-1} s^{-1}$. On the other hand, there have been few reports on solution-processed C_{60} TFT [9]. This is due to difficulty to obtain uniform and flat C_{60} layers from the solution because of the crystallization.

In this work, we demonstrated novel solution process for C_{60} thin-film layers with high field-effect mobility. We achieved highly uniform and flat C_{60} layer in selective area. C_{60} TFTs with top-contact configuration were fabricated. The highest mobility of 0.86 $cm^2 V^{-1} s^{-1}$ was obtained.

2. Experimental

Fig.1 shows C_{60} thin-film patterning process by using SAM a modified silicon substrate. A highly doped silicon wafer with a 300-nm-thick silicon oxide layer was used as a substrate. To obtain patterned C_{60} layers, we formed solution wettable and unwettable self-assembled monolayers (SAMs) on the substrate [10]. Phenyltrimethoxysilane (PTS) and hexamethyldisilazane (HMDS) were used to form wettable and unwettable SAMs, respectively. The whole area of the substrate was treated with HMDS vapor in 120°C for 10 min, and then the HMDS-SAM on selective areas was removed by UV and ozone through a metal mask. The patterned substrate was exposed to PTS vapor in 140°C for 45 min, and PTS-SAM was formed on the selective area. When the C_{60} solution was drop-casted on the whole surface of the SAM modified substrate, the solution remained only on the PTS areas. The solution on the substrate was dried in a vacuum chamber that the pressure was adjusted to 100 k, 2.7 k, or 100 Pa in 10 min. To form source/drain electrodes, an Al/LiF layer (60 nm/1 nm) was deposited through a metal mask on the patterned C_{60} layers. For the comparison, we fabricated conventional vacuum-deposited C_{60} TFTs on PTS patterned silicon substrate. Schematic illustration of the fabricated C_{60} TFT is shown in Fig.2. Transistor characteristics were measured in dry-nitrogen atmosphere.

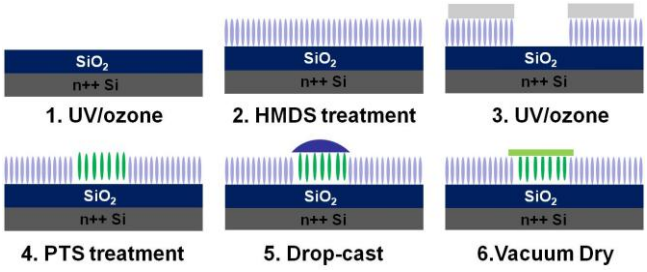

Fig.1 C_{60} thin-film patterning process

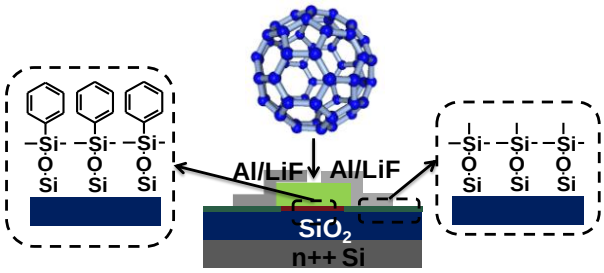

Fig.2 Schematic illustration of fabricated C_{60} TFT

3. Results

Fig.3 shows the microscopic images of (a) C_{60} solution and C_{60} solids dried at (b) 100 k (c) 2.7 k, and (d) 5 Pa on substrates with patterned PTS areas. The C_{60} solution was well patterned on the PTS area as seen in Fig.3 (a). The configuration of the dried C_{60} solid significantly depends on the pressure for the drying condition. For 100 kPa, bulky islands of C_{60} formed in the PTS area. For 2.7 kPa, many crystal-like islands of C_{60} with micron size appeared in the PTS area. This is because evaporation of solvent under low pressure promotes the nucleation of the solute in the solvent. On the other hand, for 5 Pa, uniform thin-film layers of C_{60}

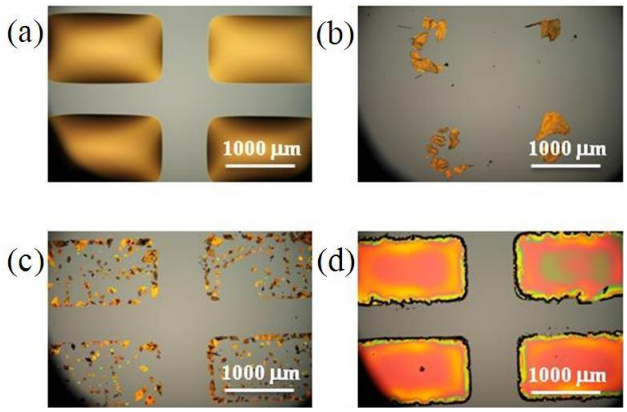

Fig.3 Optical microscopic images of (a) C_{60} solution and C_{60} solids dried at (b) 100 kPa (c) 2.7 kPa (d) 5 Pa.

were formed covering the whole PTS areas. On this condition, C_{60} molecules were readily pulled down to the substrate surface.

Fig.4 (a) and (b) show the transfer and output characteristics of a TFT with C_{60} layers dried at 5 Pa. Channel length and width were 200 μm and 1400 μm, respectively. The TFT operates as an n-channel transistor. We obtained the mobility of 0.86 $cm^2 V^{-1} s^{-1}$, and V_T of 3 V, *SS* of 0.67 V/decade, current on/off ratio of 4×10^6. The low values of V_T and *SS* are suitable for CMOS circuits with low power consumption. Since V_T and *SS* relate to trap sites between semiconductor and insulator, the result indicates that PTS-SAM is useful not only for a solution-wettable layer but also for a layer suppressing interfacial trap. Also, as it shown in Fig.4 (b), the drain current linearly increases at low drain voltages (V_D). This indicates that the FET has an ohmic-like contact, which means Al/LiF has well contact with channel layer and a matched work function.

4. Conclusions

We have demonstrated patterned and uniform C_{60} layers formed from a solution using vacuum drying process. Top-contact C_{60} FETs with Al/LiF source/drain electrodes were fabricated. The solution-processed C_{60} FET operated as an n-channel transistor and exhibited the highest mobility of 0.86 $cm^2 V^{-1} s^{-1}$. The mobility of 0.86 $cm^2 V^{-1} s^{-1}$ is the highest mobilities in the solution-processed n-channel organic FETs and even comparable for vacuum-deposited C_{60} TFTs [11]. Because the solution process using vacuum drying prevents recrystallization of small molecules, we thereby propose the application of the process to other small-molecules having a high mobility. Also with a combination of inkjet patterning technique, it is possible to fabricate high performance C_{60} TFTs in room temperature.

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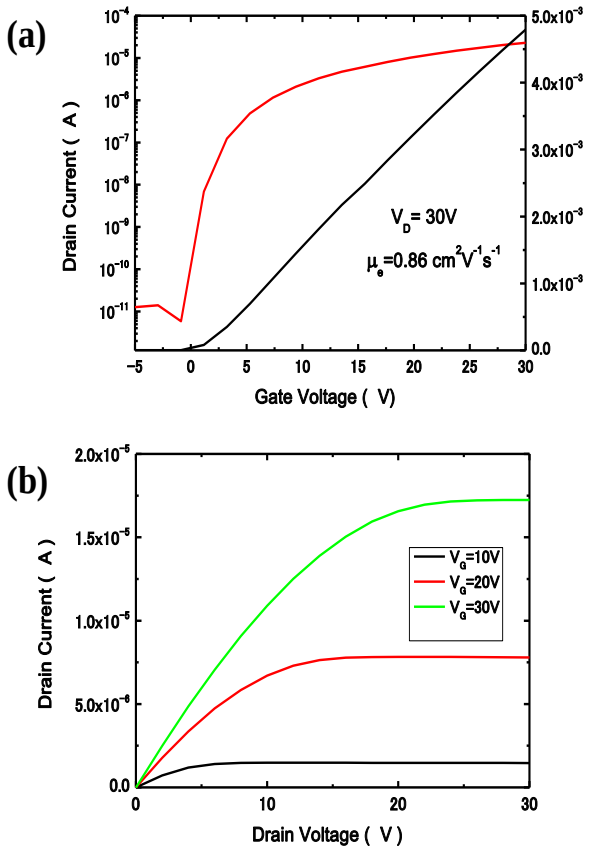

Fig.4 (a) transfer and (b) output characteristics of a solution-processed C_{60} FET. The estimated electron mobility in the saturation regime was 0.86 $cm^2 V^{-1} s^{-1}$.

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